

Curriculum Structure and Curriculum Content for the Academic Year – 2021-25

School /Department: Electronics & Communication Engineering Program: Bachelor of Engineering



Table of Contents

Vision and Mission of KLE Technological University3
Vision and Mission Statements of the School / Department4
Program Educational Objectives/Program Outcomes and Program-Specific Objectives5
Curriculum Structure-Overall7
Curriculum Structure-Semester wise9
Semester - I9
Semester - II
Semester- III
Semester- IV
Semester- V
Semester- VI
Semester- VII
Semester- VIII
List of Open Electives
List of Program Electives
Curriculum Content- Course wise19



Vision and Mission of KLE Technological University

Vision

KLE Technological University will be a national leader in Higher Education–recognised globally for innovative culture, outstanding student experience, research excellence and social impact.

Mission

KLE Technological University is dedicated to teaching that meets highest standards of excellence, generation and application of new knowledge through research and creative endeavours.

The three-fold mission of the University is:

- To offer undergraduate and post-graduate programs with engaged and experiential learning environment enriched by high quality instruction that prepares students to succeed in their lives and professional careers.
- To enable and grow disciplinary and inter-disciplinary areas of research that build on present strengths and future opportunities aligning with areas of national strategic importance and priority.
- To actively engage in the Socio-economic development of the region by contributing our expertise, experience and leadership, to enhance competitiveness and quality of life.

As a unified community of faculty, staff and students, we work together with the spirit of collaboration and partnership to accomplish our mission.



Vision and Mission Statements of the School / Department

Vision

KLE Tech-School of Electronics and Communication will be well recognized nationally and internationally for excellence in its educational programs, pioneering research and impact on the industry and society.

Mission

1. To create a unique learning environment through rigorous curriculum of theory and practice that develops students' technical, scientific, and professional skills and qualities to succeed in wide range of electronics and computing businesses and occupations.

2. To nurture spirit of innovation and state-of-the-art research to advance the boundaries of disciplinary and interdisciplinary knowledge and its applications.

3. To collaborate within and beyond the discipline to create solutions that benefit humanity and society.



Program Educational Objectives/Program Outcomes and Program-Specific Objectives

Program Educational Objectives -PEO's

1. Graduates will demonstrate peer- recognized technical competency to solve contemporary problems in the analysis, design and development of electronic devices and systems.

2. Graduates will demonstrate leadership and initiative to advance professional and organizational goals with commitment to ethical standards of profession, teamwork and respect for diverse cultural background.

3. Graduates will be engaged in ongoing learning and professional development through pursuing higher education, and self-study.

4. Graduates will be committed to creative practice of engineering and other professions in a responsible manner contributing to the socio-economic development of the society.

Program Outcomes-PO's

PO1:Engineering knowledge:

Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization for the solution of complex engineering problems.

PO 2: Problem analysis:

Identify, formulate, research literature, and analyse complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO 3:Design/Development of Solutions:

Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for public health and safety, and cultural, societal, and environmental considerations.

PO4:Conduct investigations of complex problems:

Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO 5: Modern tool usage:

Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.

PO 6: The engineer and society:



Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal, and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7: Environment and sustainability:

Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO 8: Ethics:

Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO 9: Individual and team work:

Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO 10:Communication:

Communicate effectively on complex engineering activities with the engineering community and with the society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO 11: Project management and finance:

Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12:Life-long learning:

Recognise the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Program Specific Objectives -PSO's

PSO 1: An ability to apply design principles in the development of hardware and software systems of varying complexity.

PSO 2: Demonstrate the knowledge of the state of art tools and apply for the development of VLSI circuits/systems.

PSO 3: An ability to use appropriate modern techniques for analysis, design and development of Communication components/systems.



Curriculum Structure-Overall

Semeste	r				Тс	otal Program Cred	its: 177	
	l	II	111	IV	V	VI	VII	VIII
	Single Variable Calculus 18EMAB101	Multivariable Calculus 18EMAB102	BS: Integral Transforms and Statistics 15EMAB203	BS: Linear Algebra &Partial Differential Equations 17EMAB208	PC10:CMOS VLSI Circuits 19EECC301	H3: Professional Aptitude and Logical reasoning. 23EHSA302	Wireless and Mobile Networks 24EECC403	PSE Elective 6 18EECE
de	Engineering Physics 15EPHB101	Engineering Chemistry 15ECHB102	ES1: Corporate Communication 22EHSH201	ES2:Problem Solving & Analysis 22EHSH202	PC11: Communication System 23EECC302	ES4: Industry Readiness & Leadership Skills 23EHSA304	PSE Elective 2 18EECE	Open Elective 18EECE
e with course co	Engineering Mechanics 15ECVF101	Problem Solving with Data Structures 18ECSP102	PC1: Circuit Analysis 22EECC201	ES4: Electromagnetic Fields and Waves 21EECC209	PC12: Digital Signal Processing 23EECC303	PC13:Automotive Electronics 22EECC305	PSE Elective 3 18EECE	Internship- Training 18EECI493 Internship- Project 20EECW494
Course	C Programming for Problem solving 18ECSP101	Engineering Exploration 15ECRP101	PC2: Analog Electronic Circuits 22EECC202	PC5: Linear Integrated Circuits 19EECC203	PC13: Operating System & Embedded Systems Design 22EECC304	PC14:Computer Communication Networks I 22EECC306	PSE Elective 4 18EECE	Project Work 20EECW402
	Basic Electrical Engineering 18EEEF101	Basic Electronics 18EECF101	PC3: Digital Circuits 19EECC201	PC6: Control Systems 22EECC206	PCL6: RTOS Lab 22EECP302	PSE Elective 1 17EECEXXX	PSE Elective 5 18EECE	
	Design Thinking for Social Innovation 20EHSP101	Basic Mechanical Engg. 15EMEF101	PC4: Signals & Systems 19EECC202	PC7: ARM Processor & Applications 22EECC207	PCLx: CMOS VLSI Circuits Lab 19EECP301	PCL7: Computer Communication Networks I Lab 23EECP303	P3: Senior Design Project 20EECW401	



	Engineering Physics Lab 16EPHP101	Professional Communication 15EHSH101	PCL1: Digital Circuits Lab 22EECP201	PC8: Digital System Design using Verilog 22EECC208	PC15: Machine Learning 23EECC307	PCL8: Automotive Electronics Lab 22EECP304	CIPE & EVS 15EHSA401	
			PCL2: Analog Electronic Circuits Lab 22EECP202	PCL3: Data acquisition and controls Lab 22EECP203	P1: Mini Project 23EECW301	P2: Minor Project – I 23EECW302		
			ES2: Microcontroller Architecture &Programming 22EECF202 C Programming (Dip)18EECF204	PCL4: ARM Microcontroller Lab 22EECP204	ES3:Arithmetical Thinking & Analytical Reasoning 23EHSA303	P3: Minor Project – II 23EECW303		
				PCL3: Data Structure Applications Lab 21EECF201 PCL3: Data Structure Using C Lab(Diploma) 21EECF203				
Credits	<u>21</u>	<u>23</u>	<u>25.5</u>	<u>24.5</u>	<u>23</u>	<u>22</u>	<u>21</u>	<u>17</u>



Curriculum Structure-Semester wise

Semester - I

No	Code	Course	Category	L-T-P	Credits	Contact Hours	ISA	ESA	Total	Exam Duration (in hrs)
1	18EMAB101	Single Variable Calculus	BS	4-1-0	5	6	50	50	100	3 hrs
2	15EPHB101	Engineering Physics	BS	3-0-0	3	3	50	50	100	3 hrs
3	15ECVF101	Engineering Mechanics	ES	4-0-0	4	4	50	50	100	3 hrs
4	18ECSP101	<u>C Programming for Problem</u> solving	ES	0-0-3	3	6	80	20	100	3 hrs
5	18EEEF101	Basic Electrical Engineering	ES	3-0-0	3	3	50	50	100	3 hrs
6	15EHSP101	Social Innovation	HSS	0-1-1	2	3	50	50	100	1.5hrs
7	16EPHP101	Engineering Physics Lab	BS	0-0-1	1	2	80	20	100	3 hrs
		TOTAL		14-2-5	21	27	410	290	700	



Semester - II

No	Code	Course	Category	L-T-P	Credits	Contact Hours	ISA	ESA	Total	Exam Duration (in hrs)
1	18EMAB102	Multivariable Calculus	BS	4-1-0	5	6	50	50	100	3 hrs
2	15ECHB102	Engineering Chemistry	BS	3-0-0	3	3	50	50	100	3 hrs
3	18ECSP102	Problem Solving with Data Structures	ES	0-0-3	3	6	80	20	100	3 hrs
4	15ECRP101	Engineering Exploration	ES	0-0-3	3	6	80	20	100	3 hrs
5	18EECF101	Basic Electronics	ES	4-0-0	4	4	50	50	100	3 hrs
6	15EMEF101	Basic Mechanical Engineering	ES	2-1-0	3	4	50	50	100	3 hrs
7	15EHSH101	Professional Communication	HSS	1-1-0	2	3	50	50	100	1.5 hrs
		TOTAL		14-3-6	23	32	410	290	700	



Semester- III

No	Code	Course	Category	L-T-P	Credits	Contact Hours	ISA	ESA	Total	Exam Duration (in hrs)
1	15EMAB203	BS: Integral Transforms and Statistics	BS	4-0-0	4	4	50	50	100	3 hours
2	22EHSH201	ES1: <u>Corporate</u> <u>Communication</u>	ES	0.5-0-0	0.5	1	100		100	3 hours
3	22EECC201	PC1: Circuit Analysis	PC	4-0-0	4	4	50	50	100	3 hours
4	22EECC202	PC2: Analog Electronic Circuits	РС	4-0-0	4	4	50	50	100	3 hours
5	19EECC201	PC3: Digital Circuits	PC	4-0-0	4	4	50	50	100	3 hours
6	19EECC202	PC4: Signals & Systems	ES	4-0-0	4	4	50	50	100	2 hours
7	22EECP201	PCL1: Digital Circuits Lab	PC	0-0-1	1	2	80	20	100	2 hours
8	22EECP202	PCL2: Analog Electronic Circuits Lab	РС	0-0-1	1	2	80	20	100	2 hours
9	22EECF202 18EECF204	ES2: Microcontroller Architecture & Programming C Programming (Dip)	ES	2-0-1 0-0-2	3	4	80	20	100	2 hours
		TOTAL		22.5-0-3	25.5	29	590	310	900	



Semester- IV

No	Code	Course	Category	L-T-P	Credits	Contact Hou	ISA	ESA	Total	Exam Duration (in hrs)
1	15EMAB208	BS: Linear Algebra & Partial Differential Equations	BS	4-0-0	4	4	50	50	100	3 hours
2	22EHSH202	ES2:Problem Solving & Analysis	ES	0.5-0-0	0.5	1	100		100	3 hours
3	21EECC209	ES4: Electromagnetic Fields and Waves	РС	3-0-0	3	3	50	50	100	3 hours
4	19EECC203	PC5: Linear Integrated Circuits	РС	4-0-0	4	4	50	50	100	3 hours
5	22EECC206	PC6: Control Systems	РС	4-0-0	4	4	50	50	100	3 hours
6	22EECC207	PC7: ARM Processor & Application	РС	3-0-0	3	3	50	50	100	3 hours
7	22EECC208	PC8: Digital System Design using Verilog	РС	0-0-2	2	4	80	20	100	2 hours
8	22EECP203	PCL3: Data acquisition and control Lab	РС	0-0-1	1	2	80	20	100	2 hours
9	22EECP204	PCL4: ARM Microcontroller Lab	РС	0-0-1	1	2	80	20	100	2 hours
10	21EECF201 21EECF203	PCL3: Data Structure Applications Lab PCL3: Data Structure Using C Lab(Diploma)	ES	0-0-2 0-0-3	2	4	80	20	100	2 hours
		TOTAL		18.5-0-6	24.5	31	670	330	1000	



Semester- V

Νο	Code	Course	Category	L-T-P	Credits	Contact Hours	ISA	ESA	Total	Exam Duration (in hrs)
1	19EECC301	PC10:CMOS VLSI Circuits	PC	4-0-0	4	4	50	50	100	3 hours
2	23EECC302	PC11: Communication System	PC	3-0-1	4	5	50	50	100	3 hours
3	23EECC303	PC12: Digital Signal Processing	PC	2-0-2	4	6	80	20	100	3 hours
4	22EECC304	PC13: Operating System & Embedded Systems Design	PC	3-0-0	3	3	50	50	100	3 hours
5	22EECP302	PCL6: RTOS Lab	PC	0-0-1	1	2	80	20	100	2 hours
6	19EECP301	PCLx: CMOS VLSI Circuits Lab	PC	0-0-1	1	2	80	20	100	2 hours
7	23EECC307	PC15: Machine Learning	PC	2-0-1	3	4	100		100	3 hours
8	23EECW301	P1: Mini Project	PW	0-0-3	3	6	50	50	100	2 hours
9	23EHSA303	ES3: <u>Arithmetical Thinking &</u> <u>Analytical Reasoning</u>	Audit	0-0-0		1	50	50	100	3 hours
		TOTAL		14-0-9	23	33	590	310	900	



Semester- VI

No	Code	Course	Category	L-T-P	Credits	Contact Hou	ISA	ESA	Total	Exam Duration (in hrs)
1	23EHSA302	H3: Professional Aptitude and Logical reasoning.	HC	0-0-0	Audit	3	50	50	100	3 hours
2	23EHSA304	ES4: Industry Readiness & Leadership Skills	ES	0-0-0	Audit	1	25	75	100	3 hours
3	22EECC305	PC13:Automotive Electronics	PC	3-0-0	3	3	50	50	100	3 hours
4	23EECC306	PC14:Computer Communication Networks I	PC	4-0-0	4	4	50	50	100	3 hours
5	17EECEXXX	PSE Elective 1	PE	3-0-0	3	3	50	50	100	3 hours
6	23EECP303	PCL7: Computer Communication Networks I Lab	PC	0-0-1	1	2	80	20	100	2 hours
7	22EECP304	PCL8: Automotive Electronics Lab	РС	0-0-1	1	2	80	20	100	2 hours
8	23EECW302	<u>P2: Minor Project – I</u>	PW	1-0-4	5	9	50	50	100	2 hours
9	23EECW303	<u>P3: Minor Project – II</u>	PW	0-0-5	5	10	50	50	100	2 hours
		TOTAL		11-0-11	22	37	485	415	900	



Semester- VII

No	Code	Course	Category	L-T-P	Credits	Contact Hours	ISA	ESA	Total	Exam Duration (in hrs)
1	24EECC403	Wireless and Mobile Networks	PSC	2-0-1	3	3	50	50	100	3 hours
2	18EECE	PSE Elective 2	PSE	3-0-0	3	3	50	50	100	3 hours
3	18EECE	PSE Elective 3	PSE	3-0-0	3	3	50	50	100	3 hours
4	18EECE	PSE Elective 4	PSE	3-0-0	3	3	50	50	100	3 hours
5	18EECE	PSE Elective 5	PSE	3-0-0	3	3	50	50	100	3 hours
6	20EECW401	P3: Senior Design Project	PW	0-0-6	6	12	50	50	100	3 hours
7	15EHSA401	<u>CIPE & EVS</u>	М	2-0-0	0	2	50	50	100	3 hours
		TOTAL		14-0-7	21	29	350	350	700	



Semester-VIII

No	Code	Course	Category	L-T-P	Credits	Contact Hours	ISA	ESA	Total	Exam Duration (in hrs)
1	18EECE	PSE Elective 6	PSE	3-0-0	3	3	50	50	100	3 hours
2	18EECE	Open Elective 1	OE	3-0-0	3	3	50	50	100	3 hours
3	20EECW402	Project Work	PRJ	0-0-11	11	22	50	50	100	3 hours
				O	r					
4	18EECI493 20EECW494	Internship- Training Internship- Project	PRJ PRJ	0-0-6 0-0-11	6 11	12 22	50 50	50 50	100	3 hours 3 hours
		TOTAL		6-0-11	17	28	150	150	300	

Semester	l	II	III	IV	V	VI	VII	VIII	Total
Credits	21	23	25.5	24.5	23	22	21	17	177



List of Open Electives

Sr.No	Name of the Course	Course Code
1	Automotive Electronics	18EECO403

List of Program Electives

Sr.No	Name of the Course	Course Code
1	Analog Integrated Circuit Design	23EECE301
2	Introduction to Deep Learning	23EECE322
3	Architectural Design of Integrated Circuits	23EECE302
4	Internet of Things and its Applications	23EECE307
5	Information Theory and Coding	21EECE308
6	Embedded Intelligent Systems	23EECE310
7	Multi core Architecture & Programming	23EECE340
8	OOPS using C++	23EECE321
9	9 Multimodal Machine Learning 23EECE327	
10	Digital Image Processing	23EECE328
11	System Verilog for Verification	24EECE418
12	Multimedia Communication	18EECE410
13	Physical Design-Analog	18EECE419
14	CMOS ASIC Design	24EECE420
15	AUTOSAR	20EECE406
16	Human Machine Interface	23EECE428
17	OOPS using C++	23EECE421
18	Microwave & Antennas	23EECE411
19	Wireless & Mobile Communication	24EECE432
20	Speech Processing	24EECE422
21	Product and Functional Safety	24EECE433



22	5G and Software Defined Networking	24EECE434
23	<u>GEN AI</u>	24EECE435
24	Advance IC Packaging	24EECE436
25	Digital Image Processing	23EECE414
26	MEMS	23EECE403
27	Introduction to Deep Learning	23EECE422
28	Phase-locked loops(Swayam)	22EECE432
29	VLSI Design Flow: RTL to GDS (Swayam)	23EECE435
30	Cyber Security and Privacy (Swayam)	23EECE439
31	Introduction To Algorithms And Analysis (Swayam)	23EECE440
32	Introduction to Internet of Things	24EECE446



Curriculum Content- Course wise

Program: Electronics & Commun	Semester: I				
Course Title:Single Variable Calc	Course Code:18EMAB101				
L-T-P: 4-1-0	Credits:5	Contact Hours:5 hrs/week			
ISA Marks: 50	ESA Marks: 50	Total Marks: 100			
Teaching Hours: 50Hrs	Examination Duration: 3 Hrs				

Unit I

1. Functions, Graphs and Models

Functions, types of functions, transformations and models (Linear, exponential, trigonometric). MATLAB: Graphing functions, Domain-Range and Interpreting the models

2. Calculus of functions and models

Limit of a function, Infinite limits- graph, Continuity and discontinuity, Intermediate value theorem statement, Roots of the equation using Bisection Method and Newton- Raphson Method Interpretation of derivative as a rate of change, All the rules of derivatives (List only), Maxima, Minima and optimization problems. Curvature and Radius of Curvature, Indeterminate forms, L- Hospital's rule-Examples

MATLAB: optimization problems. Curvature problems

Unit II

3. Infinite Series

Definition, Convergence of series, Tests of convergence – p-series, Alternating series. Power series, radius of convergence, Taylor's and Maclaurin's series, Applications of Taylor's and Maclaurin's series

MATLAB: Convergence of series

4. Integral calculus

Tracing of standard curves in Cartesian form ,Parametric form and Polar form; Beta and gamma function, relation between them, evaluation of integrals using Beta and gamma functions; Applications to find arc length, Area, Volume and surface area (Cartesian, parametric and polar curves). Approximate integration- Trapezoidal rule, Simpson's 1/3 rule

MATLAB: problems on arc length, area, volume and surface area

Unit III

5. Ordinary differential equations of first order

(a) Introduction to Initial Value problems. Linear and Bernoulli's equations, Exact equations and reducible to exact form, Numerical solution to Initial Value problems-Euler's method, Modified Euler's method and Runge-Kutta method

(b) Applications of first order differential equations-Orthogonal trajectories growth and decay problems, mixture problems, Electrical circuits, falling bodies.

MATLAB: Solve differential equations



Text Books:

1. Early Transcendentals Calculus- James Stewart, Thomson Books, 7ed 2010.

Reference Books:

- 1. Calculus Single and Multivariable, Hughues-Hallett Gleason, Wiley India Ed, 4ed, 2009.
- 2. Thomas Calculus, George B Thomas, Pearson India, 12ed, 2010

Back to Semester I



nication Engineering	Semester: I			
Course Title: Engineering Physics				
Credits: 3	Contact Hours:3 hrs/week			
ESA Marks: 50	Total Marks: 100			
Examination Duration: 3 Hrs				
	nication Engineering s Credits: 3 ESA Marks: 50 Examination Duration: 3 Hrs			

Unit I

Chapter 1: Conduction in semiconductors

Atomic theory: The atom, electron orbits and energy levels, energy bands, Conduction in solids: Electron motion and hole transfer, conventional current and electron flow

Conductors, semiconductors and insulators: Bonding force between atoms, Energy bands in different materials.

n-type and p-type Semiconductors: Doping, n-Type material, p-Type material, Majority and minority charge carriers, Effects of heat and light, charge carrier density.

Semiconductor conductivity: Drift current, diffusion current, charge carrier velocity, conductivity, Hall Effect.

(Text 1 Page No 1-33)

Chapter 2: Junctions

The pn-Junctions: Junction of p-Type and n-Type, Barrier voltage, depletion region, Qualitative theory of p-n Junction

Biased junctions: Reverse biased junction, forward biased junction, junction temperature effects. Junction currents and voltages: Shockley equation, junction currents, junction voltages.

p-n Junction Diode characteristics and parameters: Forward and reverse characteristics, diode parameters.

Diode approximations: Ideal diode and practical diodes, piecewise linear characteristics, DC equivalent circuits.

DC load line analysis: DC load line, Q-Point, calculating load resistance and supply voltage.

Temperature Effects: Diode power dissipation, forward voltage drop, dynamic resistance.

Diode AC models: Junction capacitance, AC-equivalent circuits (Reverse biased and forward biased), reverse recovery time.

Diode specifications: Diode data sheets, low power diodes, rectifier diodes

Diode testing: Ohmmeter tests, use of digital meter, plotting diode characteristics.

Zener diodes: Junction break down, circuit symbols and packages, characteristics and parameters, data sheet, equivalent circuits.

(Text 1 Page No 34-71)

Unit II

Chapter 3: Electrostatics

Review on vectors: Coordinate Systems, Vector and Scalar Quantities, Properties of Vectors, Components of a Vector and Unit Vectors

(Text 2 Page No 59-77)

Electric Fields: Properties of Electric Charges, Charging Objects by Induction, Coulomb's Law, Analysis Model: Particle in a Field (Electric), Electric Field of a Continuous Charge Distribution, Electric Field Lines Motion of a Charged Particle in a Uniform Electric Field

Gauss's Law: Electric Flux, Gauss's Law, Application of Gauss's Law to Various Charge Distributions, Conductors in Electrostatic Equilibrium



Electric Potential: Electric Potential and Potential Difference, Potential Difference in a Uniform Electric Field, Electric Potential and Potential Energy Due to Point Charges, Obtaining the Value of the Electric Field from the Electric Potential, Electric Potential Due to Continuous Charge Distributions Electric Potential Due to a Charged Conductor, Applications of Electrostatics Capacitance and Dielectrics: Definition of Capacitance, Calculating Capacitance, Combinations of Capacitors, Energy Stored in a Charged Capacitor, Capacitors with Dielectrics, Electric Dipole in an Electric Field, An Atomic Description of Dielectrics

(Text 2 Page No 690-807)

Unit III

Chapter 4: Electromagnetics

Magnetic Fields: Analysis Model: Particle in a Field (Magnetic), Motion of a Charged Particle in a Uniform Magnetic Field, Applications Involving Charged Particles Moving in a Magnetic Field, Magnetic Force Acting on a Current-Carrying Conductor, Torque on a Current Loop in a Uniform Magnetic Field, Sources of the Magnetic Field: The Biot–Savart Law, The Magnetic Force Between Two Parallel Conductors, Ampere's Law, The Magnetic Field of a Solenoid, Gauss's Law in Magnetism, Magnetism in Matter

Faraday's Law: Faraday's Law of Induction, Motional emf, Lenz's Law, Induced emf and Electric Fields Generators and Motors, Eddy Currents

(Text 2 Page No 868-969)

Text Book:

- 1. David A Bell, "Electronics Devices and Circuits", Fifth Edition, Oxford University Press.
- 2. Serway and Jewett, "Physics for Scientists and Engineers-with Modern Physics", 9th Edition, CENGAGE learning. 2014

Reference Books:

- 1. Jacob Millman and Christos Halkias, "Electronic Devices and Circuits" TMH
- 2. R P Feynman, Robert B Leighton, Matthew Sands, The Feynman Lectures on Physics Vol-II, Norosa Publishing House (1998).
- 3. Ben G Streetman, Solid State Electronic Devices, Prentice Hall, 1995



Program: Electronics & Commun	Semester: I			
Course Title: Engineering Mech	Course Code: 15ECVF101			
L-T-P: 4-0-0	Credits: 4	Contact Hours:4 hrs/week		
ISA Marks: 50	ESA Marks: 50	Total Marks: 100		
Teaching Hours: 50Hrs	Examination Duration: 3 Hrs			

Unit I

Chapter 1: Overview of Civil Engineering

Evolution of Civil Engineering Specialization, scope and role. Impact of Civil Engineering on National economy, environment and social & cultural fabric. Challenges and Opportunities for Civil Engineers Civil Engineering Marvels, Future challenges, Higher education and Research.

Chapter 2: Coplanar concurrent force system

Introduction to Engineering Mechanics:

Basic idealizations – Particle, Continuum, Body, Rigid body, Deformable body, Definition of force and its elements; Laws of Mechanics – Parallelogram law of forces, Principle of transmissibility, Law of Superposition, Newton's laws of motion. Classification of force systems

Resultant of coplanar concurrent force system: Definitions – Resultant, composition & Resolution of a force, Equilibrium, Equilibrant, Formulae for resultant of forces and resolution of a force. Numerical problems on resultant of forces.

Equilibrium of coplanar concurrent force system: Conditions of equilibrium, Action & Reaction, Free body diagram, Lamis' theorem. Numerical problems on equilibrium of forces.

Chapter3: Coplanar non-concurrent force system

Resultant of a force system: Moment, moment of a force, couple, moment of a couple, Characteristics of couple, Equivalent force-couple system, Numerical problems on moment of forces and couples, on equivalent force-couple system. Varignons principle of moments, Resultant of coplanar- non-concurrent force systems and numerical problems.

Unit II

Chapter4: Equilibrium of a force system (Chapter 3 contd..)

Conditions of equilibrium, types of support and loading for a statically determinate beam, Reactions at support connections, Numerical problems on equilibrium of force systems and support reactions for a statically determinate beam.

Chapter 5: Static Friction

Introduction, types of friction, definition, limiting friction, coefficient of friction, laws of Coulomb friction, angle of friction and angle of repose, cone of friction. Wedge and belt friction theory. Derivation of belt friction formula. Numerical problems on, impending motion on horizontal and inclined planes (including connected bodies); wedge friction; Ladder friction and Belt friction.

Chapter 6: Simple Stress and Strain

Introduction, Properties of Materials, Stress, Strain, Elasticity, Elastic limit, Hooke's law & Young's modulus, Stress – Strain Diagram for structural steel, working stress and Factor of safety. Deformation of a bar due to force acting on it. Law of super position. Stresses in bars of uniform & varying cross sections. Composite sections. Problems connected to above topics.

Unit III

Chapter 7: Centroid of Plane Figures

Introduction, Definition, Methods of determining the centroid, axis of reference, axis of symmetry, Locating the centroid of simple plane figures (triangle, semicircle, quarter of a circle and sector of a circle etc,.) using method of integration, Numerical problems on Centroid of simple built up sections.

KLE Technological University Creating Value, Leveraging Knowledge

Chapter 8: Second moment of area (Plane figures)

Introduction, Definition, Method of determining the second moment of area, Section Modulus, Radius of gyration, perpendicular and Parallel axis theorems, Polar second moment of area, second moment of area of simple plane figures (triangle, rectangle, semicircle, circle etc,.) using method of integration, Numerical problems on MI of simple built up sections.

Text Books:

- 1. Beer, F. P. and Johnston, R., *Mechanics for Engineers: Statics*, McGraw Hill Company, New York, 1988.
- 2. Bhavikatti, S.S., and Rajasshekarappa K.G., *Engineering Mechanics*, 3Ed., New Age International Pub. Pvt. Ltd., New Delhi, 2008.
- 3. Kumar, K.L., *Engineering Mechanics*, 3ed., Tata McGraw Hill Publishing Company, New Delhi, 2003.
- 4. Punmia, B.C., Jain, A. and Jain, A., *Mechanics of Materials*, Lakshmi Publications, New Delhi, 2006

Reference Books:

- 1. Jagadeesh, T.R. and Jayaram, *Elements of Civil Engineering*, Sapna Book House, Bangalore, 2006.
- 2. Ramamrutham, S., *Engineering Mechanics*, Dhanpat Rai Publishing Co., New Delhi, 1998.
- 3. Singer, F.L., *Engineering Mechanics*, 3rd edition Harper Collins, 1994.
- 4. Timoshenko, S.P. and Young, D.H., *Engineering Mechanics*, 4th edition, McGraw Hill Publishing Company, New Delhi, 1956.
- Irving H Shames, Engineering Mechanics, 3rd edition, Prentice-Hall of India Pvt. Ltd, New Delhi- 110 001, 1995.

Back to Semester I



Program: Electronics & Commur	nication Engineering	Semester: I	
Course Title: C Programming for	r Problem solving	Course Code: 18ECSP101	
L-T-P: 0-0-3	Credits: 3	Contact Hours:6 hrs/week	
ISA Marks: 80	ESA Marks: 20	Total Marks: 100	
Teaching Hours: 78Hrs	Examination Duration: 3 Hrs		
Introduction to Problem solving			
Introduction to algorithms/flowc	harts and its notations, top dow	n design, elementary problems.	
Basics of C programming langua	ge		
Characteristics and uses of C, Str	ucture of C program, C Tokens: k	Keywords, Identifiers, Variables,	
Constants, Operators, Data-types	s, Input and Output statements.		
Decision control statements			
Conditional branching stateme	nts: if statement, if else stat	ement, else if ladder, switch	
statement, unconditional branc	hing statements: break, contine	ue. Introduction to Debugging	
Skills Introduction to Test Driven	Programming.		
Iterative statements			
while, do while, for, nested state	ments		
Functions			
Introduction, Function declaration	on, definition, call, returns stat	ement, passing parameters to	
functions, introduction to macro	s. Introduction to Coding Standa	ards	
Arrays and Strings			
Introduction, Declaration, Acces	ssing elements, Storing values	in arrays, Operations on one	
dimensional array, Operations on	two dimensional arrays, Introdu	uction to Code Optimization and	
refactoring			
Pointers			
Introduction, declaring pointer,	pointer variables, pointer expr	ession and arithmetic, passing	
arguments to functions using po	nters, pointers and arrays, passi	ing an array to a function.	
Structures and Unions			
Introduction, passing structures	to functions, Array of structures,	, Unions	
Text Books:			
1. R. G. Dromey, How to Sol	ve it by Computer, 1ed, PHI, 200	08.	
2. Yashvant Kanetkar, Let us	C ,15 th ed, BPS Publication, 201	6.	
Reference Books:			
1. B W Kernighan, D M Ritch	nie, The Programming language	C, 2ed, PHI, 2004.	
2. B S Gottfried, Programming with C, 2ed, TMH, 2006.			
3. B. A. Forouzan, R.F. Gilb	erg, A Structured Program App	roach Using C, 3ed, CENGAGE	
Learning, 2008.			
Back to Semester I			



Program: Electronics & Commun	Semester: I		
Course Title: Basic Electrical Eng	Course Code: 18EEEF101		
L-T-P: 3-0-0 Credits: 3		Contact Hours:3 hrs/week	
ISA Marks: 50	ESA Marks: 50	Total Marks: 100	
Teaching Hours: 40Hrs Examination Duration: 3 Hrs			

Unit I

Overview of Electrical Engineering

Specialization, scope & role, impact of Electrical Engineering on national economy, environment, Sources of generation, sustainability, challenges and opportunities for electrical engineers, electrical engineering marvels, future challenges.

DC Circuits

Voltage and current sources, Kirchoff's current and voltage laws, loop and nodal analysis of simple circuits with dc excitation. Time-domain analysis of first-order RL and RC circuits.

AC Circuits

Representation of sinusoidal waveforms, peak and rms values, phasor representation, real power, reactive power, apparent power, power factor. Analysis of single-phase series and parallel R-L-C ac circuits. Three-phase balanced circuits, voltage and current relations in star and delta connections. power measurement using two watt meters

Unit II

Electrical Actuators

Electromagnetic principles, Solenoid, Relays, classification of Electric motors, DC motors-shunt, series, compound, separately excited, PMDC motors – Speed Control, Stepper Motors, BLDC motors, three phase induction motor, Characteristics and applications, selection of motors for various applications.

Power Electronics (Text1, chapter 45)

Introductory, Thyristor, Some thyristor circuits, Limitations to thyristor operation, The thyristor in practice, The fully controlled AC/DC converter, AC/DC inversion, Switching devices in inverters, Three-phase rectifier networks, The three-phase fully controlled converter, Inverter-fed induction motors, Soft-starting induction motors, DC to DC conversion switched-mode power **Unit III**

Electrical Wiring, Safety and protection (Ref :Text3-page 1 to 10)

Types of wires and cables for internal wiring, Types of switches and Circuits, Types of wiring, Safety precautions and rules in handling electrical appliances, Electric shock, first aid for electrical shocks, Importance of grounding and earthing, Methods for earthing, Fuses, MCB, ELCB and Relays, Lockout and Tagout, Electrical Codes and Standards.

Batteries

Basics of lead acid batteries, Lithium Ion Battery, Battery storage capacity, Coulomb efficiency, Numerical of high and low charging rates, Battery sizing. Numericals.



Text Books:

- 1. Hughes, Electrical & Electronic Technology, 8th , Pearson Education, 2001
- 2. P C Sen, Principals of Electrical Machines and Power Electronics, 2nd, Wiley Publications
- 3. Gilbert M Masters, Renewable and efficient Electrical Power systems, Published by John Wiley & Sons 2004 edition
- 4. Frank D. Petruzella, Electric Motors and Control Systems, McGraw Hill Education Private Limited 2009 Edition

Reference Books:

- 1. D C Kulshreshtha, Basic Electrical Engineering, Mc Graw Hill Publications
- 2. David G Alciatore and Michel B Histand, Introduction to Mechatronics and Measurement Systems, 3rd, Tata McGraw Hill Education Private Limited, New Delhi., 2005
- 3. Vincent Del Toro, Electrical Engineering Fundamentals, 2nd edition Prentice Hall India

Back to Semester I



	Program: Electronics & Communication Engineering Semes				Semeste	mester: l	
Course Title: Design Thinking for Social Innova			ion	Course Code: 20EHSP101			
L-T-P: 0-1-1		Credits: 2		Contact Hours:3 hrs/week			
ISA Marks: 80		ESA Marks: 20		Total Ma	Total Marks: 100		
	Teaching H	ours: 28H	rs	Examination Du	ration: 3 Hrs		
			 Introduc Innovati Awake conscio 	ction to Social ion: ning social ousness	Read the handout of Process of Social In by Geoff Mulgan	on "The novation"	 Class activity on Behavioral Blocks to Innovation Discussion on the behavioural blocks.
		Course sensitization	 (www. Social I Leader Engine innova (Conne Project Campu Course Studer Activit Group Activit 	Ayourstory.com) Innovation and rship eering& Social tion (EPICS) ecting SI Course to Mini t, Capstone Project, us Placements) e Overview hts' Self Introduction Y formation	 Design thinking for Social Innovation Written Assignments Writing about Akshaya Patra in class. (Background information about Akshaya patra and the Social Cuase it is addressing) Brainstorming Session on Social Innovators in Class 		 Introducing oneself with three Adjectives- Appreciating diversity and discovering self Group Formation Activity (Forming square) (Making four equilateral triangles out of popsicle sticks to enhance group cohesiveness amongst the group mates)
	KNOWLEDGE, TOOLS & DEVELOPMENT	Create Mindsets	Seven N 1. Empathy (Example of Puppies) 2. Optimism (Person Para Glass Halh fu 3. Iteration (Thomas Alw 4. Creative C (Origamy – J 5. Making it 6. Embracing (Confusion is doormat at 17 7. Learning fi (Designing V asking the st website) (Spending ou which is new	Aindsets: The Boy and the alyzed waist down / ull Half Empty) ra Edison) confidence losef Albers) g Ambiguity s the Welcome the door of Creativity) rom Failure Vebsite first and then takeholders about the ne lakh for the business rer launched)	 Handout on " Creat Mindsets" 	:e	 (How to train the Dragon? Common Video for all the mindsets) Watching in Class TED Talk on "How to build youir Creative Confidence by David Kelley – IDEO Founder)
		Process of Social Innovation	En, Cc Ide	gage ommunity study and Issue entification	Reading assignments • Handout on Com Study and Issue I • Case Study on "E • Case Study on "Jase Study on "Jas	nmunity dentification :GramSeva" anani Agri	 Activity on Observation skills To know how to use one's observation skills in understanding the social conditions

KLE Technological University Creating Value, Leveraging Knowledge

	 Class Presentations Initial observations being made by the group (Literature Survey of Places of Hubli- Dharwad) www.readwhere.com Detailed interaction / engagements with the society and finalize the social issue for intervention Use template 1: Frame your Design Challenge 	 Experience sharing by senior students Brainstorming Deliberations on the initial observations and arrive at the "Social Issue" Familiarization of the respective templates with the help of sample case study
	PEER REVIEW	
 Inspiration Plan for the Research Development of Interview guide Capture your Learnings 	Reading assignments • Handout on Overview of Inspiration Class Presentations • Entirety of the Social Issue • Identification of the Stake Holders (Examples on Fluoroscent Curtain and Students' Punctuality for Class) • Interview Questions (Role Play on Interview with Stakeholders) • Category wise Learnings capture Use template 2: Plan your Research Template 3. Development of Interview Guide	Familiarization of the respective templates with the help of sample case study
	Template 4. Capture your Learning	
 3. Ideation 3.1 Synthesis Search for meaning 	Reading assignments Handout on Overview of Idention Surthering	• Familiarization of the respective templates with the help of sample
 3. Ideation 3.1 Synthesis Search for meaning 	Reading assignments • Handout on Overview of Ideation-Synthesis	 Familiarizative respective with the handle case study



 Create "How might we" question 	Class Presentations Create insights How might we" questions Use template 5: Create Insights Template 6: Create "How Might We' Questions	
 3.0 Ideation 3.2 Prototyping Generate Ideas Select Promising Ideas Determine what to prototype Make your prototype Test and get feedback 	Reading assignments • Handout on Overview of Ideation-Prototyping Class Presentations • Story board-demonstrating the possible solutions Use template 7: Select your best ideas Template 8 : Determine what to prototype	 Brain storming Familiarization of the respective templates with the help of sample case study Activity on Risk management Activity on Resource management Structure building games
	PEER REVIEW	
 4.0 Implementation Create an action plan Community Partners (if any) Budgeting & Fundraising Peer to Peer Crowd Funding Giving Kiosks Donation Envelop Funding Marathons/ Walkathons Conducting Yoga Classes (www.causevox.com / www.blog.fundly.com) Duration Ethical concerns Launch your solution Feedback (Impact) 	Reading assignments • Handout on Overview of Implementation Class Presentations • Pilot implementation plan with required resources and Budget indicating stake holders & their enagement	Familiarization of the respective templates with the help of sample case study



5.0 Reflect Reflection of learning by t	Reading assignments ne overall • Handout on Overview of students Reflection Use template 9: Reflection on the Process Class Presentations Final Presentation- After Implementation	•	Familiarization of the respective templates with the help of sample case study

Back to Semester I



Program: Electronics & Communication Engineering		Semester: I		
Course Title: Engineering Physics lab		Course Code: 16EPHP101		
L-T-P: 0-0-1	Credits: 1	Contact Hours:2 hrs/week		
ISA Marks: 80	ESA Marks: 20	Total Marks: 100		
Teaching Hours: 24Hrs	Examination Duration: 3 Hrs			
List of Experiments				
1. Four probe method				
2. V-I characteristics of p-n junction diode				
3. Zener diode characteristics				
4. Hysteresis loss				
5. Transistor characteristics				
6. Measurement of dielectric constant				
7. Resonance frequency of LCR circuits				
8. Study of frequency response of passive components				
9. Calibration of thermocouple				
10. Calibration of electrical meters				

Back to Semester I



Program: Electronics & Communication Engineering		Semester: II
Course Title: Multivariable calculus		Course Code: 18EMAB102
L-T-P: 4-1-0	Credits: 5	Contact Hours:5 hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 50Hrs	Examination Duration: 3 Hrs	

Unit I

1. Partial differentiation

Function of several variables, Partial derivatives, Level curves, Chain rule, Errors and Approximations. Extreme value problems. Lagrange's multipliers.

2. Double integrals

Double integrals- Rectangular and polar coordinates, Change the order of integration. Change of variables, Jacobian. Application of double integrals

MATLAB: optimization problems, application of double integrals

Unit II

3. Triple integrals

Triple integrals, Cartesian, change to Cylindrical and Spherical coordinates Application of Triple integrals

4. Calculus of Vector Fields

Vector fields, Gradient and directional derivatives. Line and Surface integrals. Independence of path and potential functions. Green's theorem, Divergence of vector field, Divergence theorem, Curl of vector field. Stokes theorem.

MATLAB: application of Triple integrals, Vector calculus problems

Unit III

5. Differential equations of higher orders

 (a) Linear differential equations of second and higher order with constant coefficients The method of Variation of parameters. Initial and boundary value problems.
 (b) Applications of second order differential equations-Newton's 2nd law, electrical circuits, Simple Harmonic motion. Series solution of differential equations. Validity of Series solution of Differential equations.

MATLAB: application of differential equations

Text Books:

1. Early Transcendentals Calculus- James Stewart, Thomson Books, 7ed 2010.

Reference Books:

- 1. Calculus Single and Multivariable, Hughues-Hallett Gleason, Wiley India Ed, 4ed, 2009.
- 2. Thomas Calculus, George B Thomas, Pearson India, 12ed, 2010

Back to Semester II



Program: Electronics & Communication Engineering		Semester: II
Course Title: Engineering Chemistry		Course Code: 15ECHB102
L-T-P: 3-0-0	Credits: 3	Contact Hours:3 hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 50Hrs	Examination Duration: 3 Hrs	
L-T-P: 3-0-0 ISA Marks: 50 Teaching Hours: 50Hrs	Credits: 3 ESA Marks: 50 Examination Duration: 3 Hrs	Contact Hours: 3 hrs/week Total Marks: 100

Unit I

1. Chemical Bonding

Introduction, Ionic bond, factors influencing the formation of Ionic bond: Ionization energy. Electron affinity & electro negativity and properties of Ionic compounds. Covalent bond: Valence Bond theory & Molecular Orbital theory – formation of hydrogen molecule, factors influencing the formation of covalent bond, polar and non-polar covalent bond, dipole moment, problems on calculation of percentage of Ionic character and properties of covalent compounds, Co-ordinate bond: formation of hydronium ion and ammonium

2. Electrochemical Energy Systems

Electrode potential, Nernst equation, formation of a cell; Reference electrodes – Calomel electrode, Determination of electrode potential, numerical problems on E, $E_{cell} \& E^{0}_{cell}$. Batteries: Classification, Characteristics, Lead - acid, Lithium ion battery. Fuel cells - Methonol-O₂ fuel cell.

3. Polymers

Introduction, polymerization; mechanism of polymerization taking ethylene as an example. Determination of molecular weight of a polymer – numerical problems. Commercial polymers - Plexi glass, PS, polyurethane.

Polymer composites: Carbon fiber and Epoxy resin – synthesis, properties and applications. Introduction to conducting polymers, mechanism of conduction in poly acetylene and applications.

Unit II

4. Plating Techniques

Introduction, technological importance. Electroplating, Principles of electroplating. Factors affecting nature of electrodeposit, throwing power, Numerical problems on throwing power, Electroplating process of gold by acid cyanide bath. Electro less plating, advantages of electro less plating over electroplating. Electro less plating of Cu and its application in the manufacture of PCB.

5. Wafer Technology

Introduction, physical and chemical properties of silicon. Purification of silicon; chemical vapor deposition (CVD) process, zone refining process. Crystal growth; preparation of single crystal silicon by Czhochralski crystal pulling technique – numerical problems. Crystal slicing and wafer preparation. Fabrication process: thermal oxidation, diffusion, ion implantation – numerical problems, epitaxial growth, masking and photolithography, wet etching, dry etching.

6. Material Chemistry

Liquid Crystals – Types of liquid crystals, applications of Liquid Crystal in Display system. Fluorescence and Phosphorescence – Jablonski diagram, Thermoelectric and Piezoelectric materials – meaning, properties and applications.



Unit III

7. Instrumental methods of measurement

Advantages over conventional methods. Electro analytical methods: Potentiometer - principle, methodology and applications. Optoanalytical methods: Colorimeter - Principle, methodology and applications.

Spectral methods of analysis: UV – Spectrophotometer - Instrumentation and applications.

8. Environmental Chemistry:

Water: Sources and ill effects of water pollutants – fluoride and nitrate; determination of total hardness of water by EDTA method – numerical problems. , Sewage: Determination of Biological Oxygen Demand by Winkler's method – numerical problems and determination of Chemical Oxygen Demand – numerical problems.

Text Books:

- 1. A text Book of Engineering Chemistry, 1st edition, Dara. S. S. S. Chand & Co. Ltd., 2009, New Delhi.
- 2. A text Book of Engineering Chemistry, 16th edition, Jain P.C and Jain M, Dhanpat Rai Publications, 2006, New Delhi.

Reference Books:

- 1. Textbook of Inorganic Chemistry, P. L. Soni, Sultan Chand, 1999, New Delhi.
- 2. Hand book of batteries, David Linden, Thomas B Reddy, 3rd edition Mc Graw Hill publications, 2001, New York.
- 3. Polymer Science, 6th Edition, Gowariker V. R., Viswanathan N. V., Sreedhar J., New Age International (P) Ltd, 2007, New Delhi.
- 4. Solid State Devices& Technology, 4thEdition, V. Suresh Babu, sanguine Technical Publishers, 2005, Bangalore.
- 5. Material Science & Engineering: An Introduction, 9th Edition, Calister William D, John Wiley and sons, 2007, New York.
- 6. Instrumental methods of Chemical analysis, 5th Edition, Gurudeep R Chatwal, Shan K Anand, Himalaya Publishing House Pvt. Ltd, 2010, Mumbai.
- **7.** VLSI Technology, 2nd Edition, S. M. Sze, McGraw Hill Series in electrical and computer engineering, 1998, New York.

Back to Semester II



Program: Electronics & Communication Engineering		Semester: II		
Course Title: Problem Solving with Data Structures		Course Code: 18ECSP102		
L-T-P: 0-0-3	Credits: 3	Contact Hours:6 hrs/week		
ISA Marks: 80	ESA Marks: 20	Total Marks: 100		
Teaching Hours: 78Hrs	Examination Duration: 3 Hrs			
Pointers, Structures and Files				
Recap of basics: Pointers, Structures; Self-referential structures, dynamic memory management Files – File manipulation programs				
Stacks and Recursion				
Stack: Definition, Operations, Stack ADT Implementation of stack operations. Applications of				
stack. Recursion- Need for Recursion and problems on Recursion.				
Queues				
Queue: Definitions of Linear, Circular queues, Queue ADT Linear and circular queue operations				
Definition and working of Priority queue, Double ended queue; Applications of queues.				
Lists				
Concept of lists and dynamic memory management lists, definitions and representations: singly, doubly, circular lists. Dynamic Implementation of lists and its operations, Applications of linked lists				
Binary trees				

Binary Tree: Definition, Terminology and representation, Tree Traversals both recursive and iterative. Binary Search Tree and its applications.

Text Books:

- 1. Data Structures with C -- Seymour Lipschutz, Schaum's Outline Series
- 2. Data Structures Using C and C++ -- Langsam and Tanenbaum, PHI Publication
- 3. Data Structures Through C -- Yashavant P Kanetkar, BPB Publication

Reference Books:

- 1. B W Kernighan, D M Ritchie, The Programming language C, 2ed, PHI, 2004.
- 2. B S Gottfried, Programming with C, 2ed, TMH, 2006.
- 3. B. A. Forouzan, R. F. Gilberg, A Structured Program Approach Using C, 3ed, CENGAGE Learning, 2008.

Back to Semester II


Program: Electronics & Commur	nication Engineering	Semester: II	
Course Title: Engineering Explor	ration	Course Code: 15ECRP101	
L-T-P: 0-0-3	Credits: 3	Contact Hours:6 hrs/week	
ISA Marks: 80	ESA Marks: 20	Total Marks: 100	
Teaching Hours: 78Hrs	Examination Duration: 3 Hrs		
List of Experiments			
1. Introduction to Engineeri	ng and Engineering Study		
2. Role of Analysis in Engine	ering, Analysis Methodology		
3. Data Analysis Graphing			
4. Basics of Engineering Des	ign, Multidisciplinary Nature of	Engineering Design	
5. Project Management	5. Project Management		
6. Sustainability in Engineer	6. Sustainability in Engineering		
7. Ethics			
8. Modelling, Simulation and Data Acquisition using Software Tool			
9. Platform based development : Arduino			
10. Course Project			
Reference Books:			
1. Engineering Fundamenta	1. Engineering Fundamentals & Problem Solving by Arvid Eide, Roland Jenison, Larry		
Northup, Steven, Mc Grav	Northup, Steven, Mc GrawHill Higher Education, 6 th Edition (2011)		
2. Engineering Exploration (Engineering Exploration (Edited Book, 2008) by Pearson Publication		



Program: Electronics & Communication Engineering		Semester: II
Course Title: Basic Electronics		Course Code: 18EECF101
L-T-P: 4-0-0	Credits: 4	Contact Hours:4 hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 50Hrs Examination Duration: 3 Hrs		

Chapter 1: Trends in Electronic Industries

Introduction, Roadmap of electronic sector, scope and opportunities in various segments of electronics (i.e., Consumer, Telecom, IT, Defense, Industrial, Medical and Automobiles), Government and private sectors, Growth profile of Electronic industries, Standards and PoliISAs, Electronic System Components.

Chapter 2: Basic Components, Devices and Applications

Diode: PN junction characteristics; modeling as a circuit element, ideal and practical diode. AC to DC converter: Half wave and full wave rectifier (Centre tap and bridge), capacitor filter and its analysis, numerical examples. Zener diode and its applications (Voltage reference and voltage regulator). Realization of simple logic gates like AND and OR gates.

Chapter 3: Transistor

BJT, transistor voltages and currents, Signal amplifier (Fixed bias, Collector base bias, Voltage divider bias, CE configuration). DC load line. Voltage, current and power gains. Transistor as a switch: NOT Gate, Basic (DTL) NAND gate. Transistor as a Small Signal Amplifier (Single Stage and Two Stage RC-coupled Amplifier).

Unit II

Chapter 4: Digital Logic

Number systems: Decimal, Binary, Octal and Hexadecimal number systems, Conversions, Binary Operations-Addition and subtraction in binary number systems. Logic gates: Realization of simple logic functions using basic gates (AND, OR, NOT), Realization using universal gates (NAND, NOR). Boolean algebra: Theorems and postulates, DeMorgan's Theorems, simplification of logical expressions, Karnaugh Maps, Use of Karnaugh Maps to Minimize Boolean Expressions (2 Variables, 3 Variables and 4 Variables), Design of Half Adder and Full Adder, Parallel Adder using full adders.

Chapter 5: Operational Amplifier

OPAMP characteristics (ideal and practical), Linear and non-linear applications: Inverting amplifier, Non-inverting amplifier, Voltage follower, Integration, Differentiation, Adder, Subtractor, ZCD and Comparator.

Unit III

Chapter 6: Communication Systems

Basic block diagram of communication system, types of modulation. Amplitude modulation: Time-Domain description, Frequency-Domain description. Generation of AM wave: square law modulator. Detection of AM waves: envelope detector. Double side band suppressed carrier modulation (DSBSC), Generation of DSBSC wave: balanced modulator, Super heterodyne principle.

Chapter 7: Linear Power Supply, UPS & CRO



Working principle of linear power supply, UPS and CRO. Measurement of amplitude, frequency and phase of a given signal.

Text Books

- 1. David A Bell, Electronic devices and Circuits, PHI New Delhi, 2004
- 2. K.A Krishnamurthy and M. R. Raghuveer, Electrical, Electronics and Computer Engineering for Scientists and Engineers, 2, New Age International Publishers, 2001
- 3. A.P. Malvino, Electronic Principles, Tata McGraw Hill, 1999

Reference Books:

- 1. George Kennedy, Electronic Communication Systems, Tata McGraw Hill, 2000
- 2. Morris Mano, Digital logic and Computer design , 21st Indian print Prentice Hall India, 2000
- 3. Floyd, Digital fundamentals, 3, Prentice Hall India, 2001
- 4. Boylestead Nashelsky, Electronic devices & Circuit theory, Prentice Hall India, 2000
- 5. Ramakant Gaikawad , Operational Amplifiers & applications, PHI, 2000



Course Title: Basic Mechanical Engineering		Course Code: 15EECF101
L-T-P: 2-1-0	Credits: 3	Contact Hours:4 hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 50Hrs	Examination Duration: 3 Hrs	

Chapter 1 : Introduction to Mechanical Engineering

Definition of engineering, Mechanical Engineering, Branches of Mechanical Engineering, Who are Mechanical Engineers? Mechanical Engineers' top ten achievements. Visit to Workshop and Machine Shop, Tools, Safety Precautions Video presentations

Chapter 2: Manufacturing Engineering: Basics of Manufacturing

What is manufacturing? The main manufacturing sectors, The importance of the main manufacturing sectors to the Indian economy, Scales of production Classification of manufacturing Processes. Advances in Manufacturing: CNC machines, Mechatronics and applications. Demonstration on working of Lathe, milling, drilling, grinding machines Demonstration on Welding (Electric Arc Welding, Gas Welding, Soldering) Demonstration and Exercises on Sheet metal work. Visit to Learning Factory

Unit II

Chapter 3: Design Engineering: Power Transmission Elements

Overview

Design Application:

- Belt Drives. Types, Length of Belt. Velocity Ratio, Initial Tension. Ratio of Tensions. Power Transmitted, Numerical Problems.
- Gears. Spur Gear, Rack and Pinion, Worm Gear, Bevel Gear, Helical Gears. Speed, Torque, and Power in Gear pair. Simple and Compound Gear trains. Numerical Problems.
- Ball and Roller Bearings, Types, Applications.

Design Problems like a moving experience, aluminium can crusher Video presentations

Chapter 4: Thermal Engineering 1: Prime Movers.

Internal Combustion Engines: Classification, IC engine parts, 2 stroke SI and CI engine, 4 Stroke SI and CI Engine, PV diagrams of Otto and Diesel cycles, Comparison of 2 stroke and 4 stroke engine, comparison of CI and SI engine, Problems on Engine Performance, Future trends in IC engines. Case study on power requirement of a bike, car or any machine Video presentations **Unit III**

Chapter 5: Thermal Engineering 2: Thermal Systems' Applications

Refrigeration system, Air conditioning system, Pumps, Blowers and Compressors, Turbines, and their working principle and specifications. Case study on selection of various thermal systems Video presentations

Text Books:

- 1. Jonathan Wickert and Kemper Lewis, An Introduction to Mechanical Engineering, Third Edition, 2013- Cengage Learning.4
- 2. K. R. Gopalkrishna, Sudhir Gopalkrishna, S.C. Sharma. A Text Book of Elements of Mechanical Engineering, 30th Edition, Oct 2010,–Subhash Publishers, Bangalore.



Reference Books:

- 1. Course Material developed by the Department of Mechanical Engineering.
- 2. SKH Chowdhary, AKH Chowdhary, Nirjhar Roy, The Elements of Workshop Technology Vol I & II , 11th edition 2001, Media Promoters and Publishers.
- 3. Basic Manufacturing, Roger Timings, Third edition, Newnes, An imprint of Elsevier



Program: Electronics & Commur	nication Engineering	Semester: II
Course Title: Professional Communication		Course Code: 15EHSH101
L-T-P: 1-1-0	Credits: 2	Contact Hours:3 hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 42Hrs	Examination Duration: 3 Hrs	
	List of Experiments	
Chapter No. 1. Basics- English C	ommunication	
Course Introduction, Explana	ation of template mix-ups with	correct usages & necessity of
grammar in error detection,	Usage of tenses	
Chapter No. 2. Vocabulary and	grammar	
Vocabulary, Word Formation	and Active and Passive Voice	
Chapter No. 3. Bouncing Practic	e	
Definition, types of bouncing	, and its practice with examples,	reading skills, free style speech.
Individual presentation.		
Chapter No. 4. Rephrasing and Structures		
Comprehension and Rephras	ing, PNQ Paradigm and Structur	al practice.
Chapter No. 5. Dialogues		
Introduction of dialogues, Sit	uational Role plays.	
Chapter No. 6. Business Commu	inication	
Covering letter, formal letters, Construction of paragraphs on any given general topic.		
Reference Books:		
1. Collins Cobuild Advanced Learner's English Dictionary		
2. Raymond Murphy - Intermediate English Grammar, Cambridge University Press		

3. Martin Hewing's- Advanced English Grammar, Cambridge University Press.



Program: Electronics & Communication Engineering		Semester: III
Course Title: Integral transforms and Statistics		Course Code: 15EMAB203
L-T-P: 4-0-0	Credits: 4	Contact Hours: 4 hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 50Hrs	Examination Duration: 3 Hrs	

Chapter 1. Laplace Transforms

Definition, transforms of elementary functions- transforms of derivatives and integrals-Properties. Periodic functions, Unit step functions and Unit impulse functions. Inverse Transforms- properties- Convolution Theorem. Initial and Final value theorems, examples; Applications to differential equations, Circuit equations

Chapter 2: Probability

Definition of probability, conditional probability, Baye's rule, Chebyshev's inequality, random variables- PDF-CDF- Probability Distributions: Binomial, Poisson, Exponential, Uniform, and Normal

Unit II

Chapter 3: Regression

Introduction to method of least squares, fitting of curves y = a+bx, y = abx, correlation and regression. Engineering problems.

Chapter 4: Fourier Series

Complex Sinusoids, Fourier series representations of four classes of signals, Periodic Signals: Fourier Series representations, Derivation of Complex Coefficients of Exponential Fourier Series and Examples. Convergence of Fourier Series. Amplitude and phase spectra of a periodic signal. Properties of Fourier Series(with proof): Linearity, Symmetry Properties, Time shift, Frequency Shift, Scaling, Time differential differentiation coefficients, Time domain Convolution, Multiplication Theorem, Parseval's theorem and Examples on these properties

Chapter 6: Fourier Transform

Fourier representation of non-periodic signals, Magnitude and phase spectra. Properties of Fourier Transform: Linearity, Symmetry Properties, Time shift, Frequency Shift, Scaling, Time differential differentiation coefficients, Time domain Convolution, Multiplication Theorem, Parseval's theorem and Examples on these properties.

Unit III

Chapter 6: Random Process

- 1. Introduction to Joint Probability Distributions, marginal distribution, joint pdf and cdf, mean, variance, covariance, correlation.
- 2. Introduction to Random process, stationary process, mean, correlation and covariance function, autocorrelation function, cross correlation, Power spectral Density: properties of the spectral density; Gaussian Process: Properties of Gaussian process.

Text Books

1. Kreyszig E., Advanced Engineering Mathematics , , 10th edition, Wiley, 2015



- 2. Gupta S C and Kapoor V K, Fundamentals of Mathematical Statistics, 11th edition, Sultan Chand & Sons, 2018
- 3. Walpole and Myers, Probability and Statistics for Engineers and Scientists, ; 9thedition , Pearson Education India, 2013.

Reference Books:

- 1. Simon Haykin, Barry Van Veen, Signals and Systems Wiley; Second edition ,2007
- 2. J. Susan Milton, Jesse C. Arnold, Introduction to Probability and Statistics: Principles and
- 3. Applications for Engineering and the Computing Sciences, 4th edition, TATA Mc Graw-Hill Edition, 2017
- 4. Ian Glover & Peter Grant, Digital Communications, 3rd edition, Pearson 2009.



Program: Electronics & Communication Engineering		Semester: III
Course Title: Corporate Communication		Course Code: 22EHSH201
L-T-P: 0.5-0-0	Credits: 0.5	Contact Hours: 1 hrs/week
ISA Marks: 100	ESA Marks:	Total Marks: 100
Teaching Hours: 16Hrs Examination Duration: 3 Hrs		
Chapter No. 1. Communication Skills		

Tools of Communication, Listening, Body Language, Common Postures and Gestures, Open and Closed Body Language, Body Language to be used in Corporate Scenarios, Voice: Pitch, Pace, and Pause, Verbal Language: Positive & Negative Vocabulary, Corporate Conversations

Chapter No. 2. Presentation Skills

Zero Presentation, Individual Presentations, and feedback, Making Presentations Interactive, Types of Questions, Taking off and Signing off differently, Captivating your Audience, Corporate Presentations

Chapter No. 3. Spoken English

Phonetic and Non-Phonetic Languages, Introduction to IPA, Sounds in English, Syllables, Word Stress, Rhythm, Pausing, and Intonation

Chapter No. 4. Written English

Vocabulary Enhancement Strategies, Root Words in English, Grammar Improvement Techniques, Dictionary Usage, Similar and Contradictory Words

Reference Books:

- 1. Diana Booher Communicate With Confidence, Mc Graw Hill Publishers
- 2. Norman Lewis Word Power Made Easy, Goyal Publishers
- 3. Cambridge Advanced Learner's Dictionary, Cambridge University Press.



Program: Electronics & Communication Engineering		Semester: III
Course Title: Circuit Analysis		Course Code: 22EECC201
L-T-P: 4-0-0	Credits: 4	Contact Hours: 4 hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 50Hrs	Examination Duration: 3 Hrs	

Chapter 1: Basics

Active and passive circuit elements, Voltage & current sources, Resistive networks, Nodal Analysis, Super node, Mesh Analysis, Super mesh, Star – Delta Transformation. [Text 1: Chapter 4,5, 7]

Chapter 2: Network Theorems

Homogeneity, Superposition and Linearity, Thevenin's & Norton's Theorems, Maximum Power Transfer Theorem, Miller's theorem, Reciprocity principle.

[Text 1 : Chapter 5]

Chapter 3: Network topologies

Graph of a network, Concept of tree and co-tree, incidence matrix, tie set and cut set schedules, Formulation of Equilibrium equations in matrix form, Solution of resistive networks.[Text 1: Chapter 5]

Unit II

Chapter 4: Two Port Networks

Two port variables, Z, Y, H, G, A - Parameter representations, Input and output impedance calculation, Series, Parallel and Cascade network connections, and their (suitable) models. [Text 2 : Chapter 11]

Chapter 5: Time and Frequency domain Representation of Circuits

Order of a system, Concept of Time constant, System Governing equation, System Characteristic equation, Initial conditions, Transfer Functions (Fourier and Laplace domain representation) [Text 2: Chapter 4]

Chapter 6: First order circuits

Transient response of R-C and R-L networks (with Initial conditions) Concept of phasor, Phasor diagrams, Frequency response characteristics, Polar plots R-C, R-L circuits as differentiator and integrator models, time and frequency domain responses RC, R-L circuits as Low pass and high pass filters

[Text 2: Chapter 5, Text 1: Chapter 8,9,10]

Unit III

Chapter No. 7. Higher order circuits

Higher order R-C, R-L, and R-L-C networks, time domain and frequency domain representation, Series R-L-C circuit, Transient response, Damping factor, Performance parameters, Quality factor, Frequency response curve, Peaking of frequency curve and its relation to damping factor. Series and Parallel Resonance, Quality factor, Selectivity and Bandwidth

[Text 2: Chapter 7,8] [Text 1: Chapter 4,5, 7]

Text Books:



- 1. W H Hayt, J E Kemmerly, S M Durban, "Engineering Circuit Analysis" McGraw Hill Education; Eighth edition ,2013
- 2. M E. Van Valkenburg, Network Analysis, Third edition Pearson Education, 2019

Reference Books:

- 1. Joseph Edminister, Mahmood Nahavi, Electric Circuits, 5th edition, McGraw Hill Education, 2017
- 2. V. K. Aatre, —Network Theory and Filter Design,3rd edition, New Age International Private Limited,2014



Program: Electronics & Communication Engineering		Semester: III
Course Title: Analog Electronic Circuits		Course Code: 22EECC202
L-T-P: 4-0-0	Credits: 4	Contact Hours:4 hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 50Hrs Examination Duration: 3 Hrs		

Chapter 1:Diode Models and Circuits

Recap of diode models: Exponential model, piece-wise linear model, constant voltage drop model, ideal diode model, small signal diode model and derivation of small signal diode resistance. Applications of diodes as a Clipping and clamping circuits with and without DC bias voltage; Voltage doublers Numericals on applications. (T1: 2.2, 2.3.1 to 2.3.8, 2.6.1 to 2.6.3.)

Chapter 2: Bipolar junction transistors

Recap of DC load line and bias point, Small signal operation-the transfer characteristics, the amplifier gain, and operation as a switch. Biasing of BJT: voltage divider, Small signal models of bipolar transistors, two port modelling of amplifiers, H-model, ac analysis of BJT circuits-coupling and bypass capacitor, Common emitter circuit analysis without RE resistance(Emitter resistor) Numericals on amplifiers and switch. (T1: 3.2.1,3.2.2, 3.2.3, 3.2.4, 3.3.1, 3.3.2, 3.3.4)

Chapter 3: MOSFETs structure and physical operation:

MOSFET Device structure, NMOS :Depletion type ; operation with no gate voltage, positive and negative gate voltage and Enhancement type ; operation with no gate voltage, positive and negative gate voltage creating a channel for current flow, applying small vds, operation as vds is increased, Derivation of threshold voltage of MOSFET, Operating the MOS transistor in the sub threshold region, Pinch off effect , channel length modulation effect , derivation of the ID-VDS relationship, with and without channel length modulation. Finite output resistance (rds on) in saturation, PMOS: Drain and Transfer characteristics, circuit symbol, the ID v/s VDS characteristics, and the role of the substrate-the body effect, temperature effects, breakdown and input protection. Threshold Voltage Derivation MOSFET circuits at DC.

Unit II

Chapter 4: Biasing of MOSFETs

MOSFET circuits at DC continued. Biasing in MOS amplifier circuits,: By fixing VGS; By fixing VG; With drain to gate feedback resistor; Constant current source biasing, MOSFET as a switch Large – signal operation, operation as a linear amplifier and Numericals. (T1:4.3)

Chapter 5: MOSFET amplifiers

Small signal operation and models, single stage MOS amplifiers, the MOSFET internal capacitance, Derivation of CS, CG and CD amplifiers parameters and its comparison, Implications on gain and Bandwidth. Source degenerated common source amplifier, cascade and cascaded circuits High frequency model of the MOSFET, revision of common-gate, common- source, common-drain circuits; poles and zeros in the transfer function (T1:4.4,4.5, 4.6.1 to 4.6.7; 4.7.1, 4.7.2, 4.7.3, 4.7.5, 4.7.6, 4.7.7; 4.8.1, 4.8.2, 4.8.3, 4.8.4, 4.9.1 to 4.9.3)

Unit III

Chapter 6: Feedback Amplifiers :



General feedback structure (Block schematic), Feedback desensitivity factor, positive and negative feedback Nyquist stability Criterion, RC phase shift oscillator, wein bridge Oscillator, merits of negative feedback, feedback topologies: series-shunt feedback amplifier, series-series feedback amplifier, and shunt-shunt and shunt-series feedback amplifier with examples (T1:7.1 to 7.6)

Chapter 7: Large Signal Amplifiers :

Classification of amplifiers: (A, B, AB and C); Transformer coupled amplifier, push-pull amplifier Transistor case and heat sink. (T1:12.1 to 12.6;12.8.4)

Text Books

1. A.S. Sedra& K.C. Smith, "Microelectronic Circuits",7th edition, Oxford University Press, 2017

Reference Books:

- Jacob Millman and Christos Halkias,—Integrated Electronics "McGraw Hill Education, 2nd edition 2017
- 2. David A. Bell,—Electronic Devices and Circuits, Oxford Fifth edition 2008
- 3. Grey, Hurst, Lewis and Meyer,—Analysis and design of analog integrated circuits,Wiley,5th edition 2009
- 4. Thomas L. Floyd,—Electronic devices ,Pearson, 10th edition, 2018
- 5. Richard R. Spencer & Mohammed S. Ghousi, Introduction to Electronic Circuit Design ||, Pearson Education, 2003
- 6. J. Millman& A. Grabel, "Microelectronics"-2nd edition, McGraw Hill, 2017
- 7. Behzad Razavi,—Fundamentals of Microelectronics, 2nd edition Wiley;2013



Program: Electronics & Communication Engineering		Semester: III
Course Title: Digital Circuits		Course Code: 19 EECC201
L-T-P: 4-0-0	Credits: 4	Contact Hours: 4 hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 50Hrs Examination Duration: 3 Hrs		
Unit I		

Chapter No. 1. Logic Families

Logic levels, output switching times, fan-in and fan-out, comparison of logic families

Chapter No. 2. Principles of Combinational Logic

Definition of combinational logic, canonical forms, Generation of switching equations from truth tables, Karnaugh maps-3,4 variables, Incompletely specified functions(Don't care terms), Simplifying Maxterm equations, Quine-McCluskey minimization technique- Quine-McCluskey using don't care terms, Reduced Prime Implicant Tables.

Chapter No. 3. Analysis and design of combinational logic

General approach, Decoders-BCD decoders, Encoders, Digital multiplexers- Using multiplexers as Boolean function generators. Adders and subtractors-Cascading full adders, Look ahead carry adders, Binary comparators.

Unit II

Chapter No. 4.Introduction to Sequential Circuits

Basic Bistable Element, Latches, A SR Latch, Application of SR Latch, A Switch De bouncer, The SR Latch, The gated SR Latch, The gated D Latch, The Master-Slave Flip-Flops (Pulse-Triggered Flip-Flops): The Master-Slave SR Flip-Flops, The Master-Slave JK Flip-Flop, Edge Triggered Flip- Flop: The Positive Edge-Triggered D Flip-Flop, Negative-Edge Triggered D Flip-Flop; Characteristic Equations

Chapter No. 5. Analysis of Sequential Circuits

Registers and Counters, Binary Ripple Counters, Synchronous Binary counters, Ring and Johnson Counters, Design of a Synchronous counters, Design of a Synchronous Mod-n Counter using clocked JK Flip-Flops Design of a Synchronous Mod-n Counter using clocked D, T or SR Flip-Flops. **Unit III**

Chapter No. 6. Sequential Circuit Design

Introduction to Sequential Circuit Design, Mealy and Moore Models, State Machine notations, Synchronous Sequential Circuit Analysis, Construction of state Diagrams and counter design.

Chapter No. 7. Introduction to memories

Introduction and role of memory in a computer system, memory types and terminology, Read Only memory, MROM, PROM, EPROM, EEPROM, Random access memory, SRAM, DRAM, NVRAM.

Text Books

- 1. Donald D Givone, Digital Principles and Design, McGraw Hill Education ,2017
- John M Yarbrough, Digital Logic Applications and Design, 1st edition Cengage Learning, 2006

3. A Anand Kumar, Fundamentals of digital circuits 4th Revised edition, PHI ,2016 **Reference Books:**



- 1. Charles H Roth, Fundamentals of Logic Design,7th edition ,Cengage Learning, 2015
- 2. ZviKohavi, Switching and Finite Automata Theory Cambridge University Press; 3rd edition October 2009
- 3. R.D. Sudhaker Samuel, Logic Design, Pearson Education ,2010
- 4. R P Jain, Modern Digital Electronics ,4th edition, McGraw Hill Education,2009



Program: Electronics & Communication Engineering		Semester: III
Course Title: Signals and Systems		Course Code: 19EECC202
L-T-P: 4-0-0	Credits: 4	Contact Hours:4 hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 50Hrs	Examination Duration: 3 Hrs	

Chapter No. 01: Signal Representation

Definition of a signals and systems, classification of signals, (analog and discrete signal, periodic and aperiodic, deterministic and random signals, even and odd signals, energy and power), basic operation on signals (independent variable, dependent variable, time scaling, multiplication, time reversal), elementary signals (Impulse, step, ramp, sinusoidal, complex exponential), Systems Interconnections (series, parallel and cascade), properties of linear systems. (homogeneity, superposition, linearity and time invariance, stability, memory, causality)

Chapter No. 02 : LTI System Representation

Impulse response representation and properties, Convolution, convolution sum and convolution integral. Differential and difference equation Representation, Block diagram representation

Unit II

Chapter No. 03: Fourier representation for signals

Introduction, Discrete time Fourier series (derivation of series excluded) and their properties. Discrete Fourier transform (derivation of transform excluded) and properties

Chapter No. 04: Applications of Fourier transform

Introduction, frequency response of LTI systems, Fourier transform representation of periodic signals, Fourier transform representation of discrete time signals. Sampling of continuous time signals.

Unit III

Chapter No. 05: Z-transform

Definition of z-transform, Properties of ROC, Properties of Z-transforms: Inverse z-transforms (Partial Fraction method, long division method), Unilateral Z-transform, Transform of LTI.

Text Books

- 1. Simon Haykin and Barry Van Veen, Signals and Systems, 2nd edition Wiley, 2007
- 2. Alan V Oppenheim, Alan S Willsky and S. Hamid Nawab, Signals and Systems, Second, PHI public,1997

Reference Books:

- 1. H. P Hsu, R. Ranjan, Signals and Systems ,; 2nd edition, McGraw Hill ,2017
- 2. Ganesh Rao and SatishT unga, Signals and Systems 1st edition, Cengage India, 2017
- 3. M. J. Roberts, Fundamentals of Signals and Systems 2nd edition, McGraw Hill Education, 2017



Program: Electronics & Communication Engineering		Semester: III
Course Title: Digital Circuits Laboratory Experiments		Course Code: 22EECP201
L-T-P: 0-0-1	Credits: 1	Contact Hours:2 hrs/week
ISA Marks: 80	ESA Marks: 20	Total Marks: 100
Teaching Hours: Examination Duration: 2 Hrs		
List of Experiments:		

- 1. Characterization of TTL Gates- Propagation delay, Fan-in, Fan-out and Noise Margin.
- 2. To verify of Flipflops (a) JK Master Slave (b) T-type and (c)D-Type
- 3. Design and implement binary to gray, gray to binary, BCD to Ex-3 and Ex-3 to BCD code converters.
- 4. Design and implement BCD adder and Subtractor using 4 bit parallel adder.
- 5. Design and implement n bit magnitude comparator using 4- bit comparators.
- 6. Design and implement Ring and Johnson counter using shift register.
- 7. Design and implement 8:3 Priority Encoder
- 8. Design and implement frequency divider
- 9. Design and implement mod-6 synchronous and asynchronous counters using flip flops.
- 10. Design and implement given functionality using decoders and multiplexers.
- 11. Design and implement a digital system to display a 3 bit counter on a 7 segment display. Demonstrate the results on a general purpose PCB.

**Note-All above experiments are to be conducted along with simulation.

**Digital Circuits Lab:* Simulation of combinational and sequential circuits using netlist based Spice Simulators (Avoid using drag n drop), before implementing the circuits on breadboard.

Reference Books:

- 4. K. A. Krishnamurthy-Digital lab primer ||, Pearson Education Asia Publications, 2003.
- 5. A.P. Malvino, -Electronic Principles 7th edition, McGraw Hill Education, 2017



Program: Electronics & Communication Engineering		Semester: III
Course Title: Analog Electronics Laboratory Experiments		Course Code: 22EECP202
L-T-P: 0-0-1	Credits: 1	Contact Hours:2 hrs/week
ISA Marks: 80	ESA Marks: 20	Total Marks: 100
Teaching Hours:	Examination Duration: 2 Hrs	

List of Experiments:

- 1. Study of multi-meters, power supplies, function generators, Oscilloscopes; Identification of various components and devices, e.g. resistors, capacitors, diodes, transistors.
- 2. Design & analyze Diode Clipping circuits.
- 3. Design & analyze Positive and Negative Clamping circuits.
- 4. Study of BJT as a Switch.
- 5. Study the input and output characteristics of MOSFET.
- 6. To study the basic current mirror circuit.
- 7. MOSFET as a source follower (Buffer).
- 8. Study of transformer-less Class B push pull power amplifier and determination of its conversion efficiency
- 9. Design an amplifier using BJT and determine its gain, input, output impedance and frequency response of RC Coupled single stage BJT amplifier
- 10. Design an amplifier using MOSFET and determine its gain, input, output impedance and frequency response of a CS amplifier.
- 11. Design a regulated power supply for the given specifications

**Note-All above experiments are to be conducted along with simulation.

*Analog Electronic Circuits Lab: Simulation of designed circuits using LTSpice Simulator, before implementing the circuits on breadboard.

Reference Books:

- "Electronic Devices & circuit Theory" by Nashelsky & Boylstead, 11th Edition, Pearson, 2015
- "Integrated Electronics"–By Jacob Millman and Christos Halkias ,McGraw Hill Education; 2nd edition 2017
- 3. "Electronic Principles" by A.P. Malvino, 7thedition, McGraw Hill Education, 2017



Program: Electronics & Communication Engineering		Semester: III
Course Title: Microcontroller Architecture & Programming		Course Code: 22EECF202
L-T-P: 2-0-1	Credits: 3	Contact Hours: 2 hrs/week
ISA Marks: 80	ESA Marks: 20	Total Marks: 100
Teaching Hours: 30Hrs	Examination Duration: 2 Hrs	

Chapter 1: Microprocessors and microcontroller

Introduction, Microprocessors and Microcontrollers, A Microcontroller Survey, RISC & CISC CPU Architectures, Harvard & Von-Neumann CPU architecture.

Chapter 2: The 8051 Architecture

8051 Microcontroller Hardware, Input / Output Pins, Ports and Circuits, semiconductor Memories, Interfacing external RAM & ROM memories.

Chapter 3: Addressing Modes and Arithmetic Operations

Addressing modes, External data Moves, Code Memory, Read Only Data Moves / Indexed Addressing mode, Data exchanges, stack concept and related instructions, example programs. Logical Operations: Introduction, Byte level, logical Operations, Bit level Logical Operations , Rotate and Swap Operations, Example Programs, Arithmetic Operations: Introduction, Flags, Incrementing and Decrementing, Addition, Subtraction Multiplication and Division, Decimal Arithmetic, Example Programs.

Unit II

Chapter 4 Branch operations

Jump Operations: Introduction, The JUMP and CALL, Program range, Jump calls and Subroutines, Interrupts and Returns, Example Problems.

Chapter 5: 8051 Programming in 'C'

Data Types and Time delays in 8051C, I/O Programming, Logic operations, Data Conversion programs, Accessing code ROM space, Data serialization.

Chapter 6: Counter/Timer Programming in 8051

Programming 8051 Timers, Programming Timer0 and Timer1 in 8051C

Unit III

Chapter 7: Serial Communication

Basics of Serial Communication, 8051 connections to RS-232,8051 Serial Communication modes, Programming, Serial port programming in C.

Chapter 8: 8051 interfacing and applications

Interfacing 8051 to LCD, Keyboard, ADC, DAC, Stepper Motor, DC Motor.

Chapter 9: Interrupts



Introduction to interrupts, interrupts vs polling, classification of interrupts, interrupt priority, interrupt vector table, interrupt service routine

Text Books

- 1. "The 8051 Microcontroller Architecture, Programming & Applications" by 'Kenneth J. Ayala', Penram International, 1996
- 2. "The 8051 Microcontroller and Embedded systems", by ' Muhammad Ali Mazidi and Janice Gillispie Mazidi', Pearson Education, 2003

Reference Books:

1. "Programming and Customizing the 8051 Microcontroller", by 'Predko', TMH.



Program: Electronics & Communication Engineering		Semester: III		
Course Title: C Programming (for Diploma) Course Cou		e: 18EECF204		
L-T-P: 0-0-2	T-P: 0-0-2 Credits: 2 Contact Ho		urs:4 hrs/week	
ISA Marks: 80	A Marks: 80 ESA Marks: 20 Total Marks		: 100	
Teaching Hours	5:	Examination Duration: 2 Hrs		
1. <u>List</u>	of experiments/j	obs planned to meet the requir	ements of th	<u>e course.</u>
Expt./Job		Experiment/job Details		No. of Lab.
No.				Session/s per
				batch
				(estimate)
1	Write a C progra	m to perform addition subtrac	tion	01
1.	write a c progra	ad division of two numbers	uon,	01
	inultiplication al	id division of two numbers.		
1.	Write a C progra	im to		01
	i) Ident	ify greater number between tw	vo numbers	
	, using	C program.		
	ii) To ch	eck a given number is Even or C)dd.	
2.	Write a C progra	im to		01
	 i) To find the roots of a quadratic equation. ii) Find the factorial of given purchase 			
	II) Find the factorial of given number.			
3.	Write a C progra	im to		01
	i) To fir	nd the sum of n natural numbers	s.	
	ii) Print	the sum of 1 + 3 + 5 + 7 + + n		
4.	Write a C	C program to		01
	i) Print the pattern.			
	*			
	* *			
	* * *			
	* * * *			
	* * * *			
	ii) Print the pattern			
	1			
	12			
	123			

KLE Technological University Creating Value, Leveraging Knowledge

	1234	
	12345	
6.	Write a C program to	01
	To test whether the given character is Vowel or not. (using switch case)	
7.	Write a C program to	01
	To accept 10 numbers and make the average of the	
	numbers using one dimensional array.	
8.	Write a C program to	01
	Find out square of a number using function.	
9	Write a C program to	01
	To find the summation of three numbers using function.	
10	Write a C program to	01
	Find out addition of two matrices.	
1. Materia	als and Resources Required:	
Text Book		
1. Programming in ANSI C, E Balagurusamy		



Program: Electronics & Communication Engineering		Semester: IV
Course Title: Linear Algebra and Partial Differential		Course Code: 15EMAB208
Equations		
L-T-P: 4-0-0	Credits: 4	Contact Hours:
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 50Hrs	Examination Duration: 3 Hrs	

Chapter1: Partial differential equations

Introduction, classification of PDE, Formation of PDE, Solution of equation of the type Pp + Qq = R, Solution of partial differential equation by direct integration methods, method of separation of variables. modelling: Vibration of string-wave equation, heat equation. Laplace equation. Solution by method of separation of variables.

Chapter2: Finite difference method

Finite difference approximations to derivatives, finite difference solution of parabolic PDE, explicit and implicit methods; Hyperbolic PDE-explicit method, Elliptic PDE-initial-boundary Value problems..

Unit II

Chapter3: Fourier Series

Complex Sinusoids, Fourier series representations of four classes of signals, Periodic Signals: Fourier Series representations, Derivation of Complex Co- efficient of Exponential Fourier Series and Examples. Convergence of Fourier Series. Amplitude and phase spectra of a periodic signal. Properties of Fourier Series (with proof): Linearity, Symmetry Properties, Time shift, Frequency Shift, Scaling, Time differential differentiation coefficients, Time domain Convolution, Multiplication Theorem, Parseval's theorem and Examples on these properties.

Chapter 4: Fourier Transform

Fourier representation of non-periodic signals, Magnitude and phase spectra. Properties of Fourier Transform: Linearity, Symmetry Properties, Time shift, Frequency Shift, Scaling, Time differential differentiation coefficients, Time domain Convolution, Multiplication Theorem, Parseval's theorem and Examples on these properties.

Unit III

Chapter5: Complex analysis

Function of complex variables. Limits, continuity and differentiability. Analytic functions, C-R equations in Cartesian and polar forms, construction of Analytic functions (Cartesian and polar forms).

Chapter 7: Complex Integration

Line integral, Cauchy's theorem- corollaries, Cauchy's integral formula. Taylor's and Laurent Series, Singularities, Poles, Residue theorem – problems.

Text Books

1. Simon Haykin, Barry Van Veen, Signals and Systems, 2ndedition, Wiley, 2007



- 2. Peter V. O'neil, Advanced Engineering Mathematics Cengage Learning Custom Publishing; 7th Revised edition2011
- 3. Dennis G Zilland Michael R Cullin,"Advanced Engineering Mathematics",4th edition, NarosaPublishingHouse,NewDelhi,2012

Reference Books:

- 1. Kreyszig E., Advanced Engineering Mathematics, 10th edition, Wiley, 2015
- 2. Stanley J Farlow, Partial differential equations for Scientists and Engineers, Dover publications, INC, New York, 1993



Program: Electronics & Commur	ication Engineering	Semester: IV	
Course Title: Problem Solving & Analysis		Course Code: 22EHSH202	
L-T-P: 0.5-0-0	Credits: 0.5	Contact Hours: 1 hrs/week	
ISA Marks: 100	ESA Marks:	Total Marks: 100	
Teaching Hours: 16Hrs	Examination Duration: 3 Hrs		
Chapter No. 1. Analytical Thinki	ng		
Analysis of Problems, Puzzles	for practice, Human Relations	, Direction Tests; Looking for	
Patterns: Number and Alphabet	Series, Coding Decoding; Diagra	mmatic Solving: Sets and Venn	
diagram-based puzzles; Visual Re	asoning, Clocks and Calendars		
Chapter No. 2. Mathematical Th	ninking		
Number System, Factors and N	Iultiples, Using Simple Equatio	ns for Problem Solving, Ratio,	
Proportion, and Variation			
Chapter No. 3. Verbal Ability			
Problem Solving using Analogies,	Sentence Completion		
Chapter No. 4. Discussions & Debates			
Team efforts in Problem Solving; A Zero Group Discussion, Mock Group Discussions, and			
Feedback; Discussion v/s Debate	; Starting a Group Discussion: Re	cruitment and other Corporate	
Scenarios; Evaluation Parameters in a Recruitment Group Discussion, Types of Initiators: Verbal			
and Thought, Conclusion of a Discussion			
Reference Books:			
1. R. S. Aggarwal, "A Modern Approach to Verbal and Non – Verbal Reasoning", Sultan			
Chand and Sons, New Delhi, 2018			
2. R. S. Aggarwal, "Quantitative Aptitude", Sultan Chand and Sons, New Delhi, 2018			
Chopra, "Verbal and Non – Verbal Reasoning", MacMillan India			
4. M Tyra, "Magical Book or	M Tyra, "Magical Book on Quicker Maths", BSC Publications, 2018		
5. Diana Booher - Communi	cate With Confidence, Mc Graw	Hill Publishers	
6. Norman Lewis–Word Pow	6. Norman Lewis–Word Power Made Easy, Goyal Publishers		
7. Cambridge Advanced Lea	7. Cambridge Advanced Learner's Dictionary, Cambridge University Press.		
8. Kaplan's GRE guide	8. Kaplan's GRE guide		



Program: Electronics & Communication Engineering		Semester: IV
Course Title: Electromagnetic Fields and Waves		Course Code: 21EECC209
L-T-P: 3-0-0	Credits: 3	Contact Hours:3 hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 40Hrs	Examination Duration: 3 Hrs	

Chapter No. 1. Electrostatic Fields

Introduction, Coulomb's Law and Field Intensity, Electric Fields Due to Continuous Charge Distribution, Electric Flux Density, Gauss's Law – Maxwell's Equation, Application of Gauss's Law, Electric Potential, Relationship between E and V – Maxwell's Equation, An Electric Dipole and Flux Lines, Energy Density in Electrostatic Fields.

Chapter No. 2. Electric Fields in Material Space

Introduction, Properties of materials, Convection and Conduction Currents, Conductors, Polarization in Dielectrics, Dielectric Constant and strength, Continuity Equation and Relaxation Time, Boundary Conditions.

Chapter No. 3. Electrostatic Boundary-Value Problems

Introduction, Poisson's and Laplace's Equations, Uniqueness Theorem, General Procedure for Solving Poisson's or Laplace's Equation, Resistance and Capacitance, Method of Images.

Unit II

Chapter No. 4. Magnetostatic Fields

Introduction, Biot-Savart's Law, Ampere's Circuit Law—Maxwell's Equation, Applications of Ampere's Law, Magnetic Flux Density—Maxwell's Equation, Maxwell's Equations for Static EM Fields, Magnetic Scalar and Vector Potentials, Derivation of Biot-Savart's Law and Ampere's Law.

Chapter No. 5. Magnetic Forces, Materials and Devices

Introduction, Forces due to Magnetic Fields, Magnetic Torque and Moment, A Magnetic Dipole, Magnetization in Materials, Classification of Magnetic Materials, Magnetic Boundary Conditions, Inductors and Inductances, Magnetic Energy, Magnetic Circuits, Force on Magnetic Materials **Chapter No. 6. Maxwell's Equations**

Introduction, Faraday's Law, Transformer and Motional Electromotive Forces, Displacement Current, Maxwell's Equations in Final Forms, Time-Varying Potentials, Time-Harmonic Fields.

Unit III

Chapter No. 7. Electromagnetic Wave Propagation

Introduction, Wave Propagation in Lossy Dielectrics, Plane Waves in Lossless Dielectrics, Plane Waves in Free Space, Plane Waves in Good Conductors, Power and the Poynting Vector, Reflection of a Plane Wave at Normal Incidence, Reflection of a Plane Wave at Oblique Incidence.

Chapter No. 8. Transmission Lines

Introduction, Transmission Line Parameters, Transmission Line Equations, Input Impedance, SWR, and Power, The Smith Chart, Transients on Transmission Lines, Microstrip Transmission Lines, Some Applications of Transmission Lines.

Text Books

- 1. William Hayt. Jr. John A. Buck, Engineering Electromagnetics 9th edition, McGraw Hill Education, 2018.
- 2. R. K. Shevgaonkar, Electromagnetic Waves McGraw Hill Education; 1st edition, 2017
- 3. Mathew N. O. Sadiku, Elements of Electromagnetics; Sixth edition, Oxford University, 2015





Program: Electronics & Communication Engineering		Semester: IV
Course Title: Linear Integrated circuits		Course Code: 19EECC203
L-T-P: 4-0-0	Credits: 4	Contact Hours:4 hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 50Hrs	Examination Duration: 3 Hrs	

Chapter No 1. Current Mirrors

Current Mirror circuits, Current source and current sink, Figures of merit (output impedance, voltage swing), Widlar, Cascade and Wilson current Mirrors.

Chapter No 2. Basic OPAMP architecture

Basic differential amplifier, Common mode and difference mode gain, CMRR, 5-pack differential amplifier with design, 7-pack operational amplifier, Slew rate limitation, Bandwidth and frequency response curve.

Chapter No 3. OPAMP characteristics

Ideal and non-ideal OPAMP terminal characteristics, Input and output impedance, output Offset voltage, Small signal and Large signal bandwidth.

Unit II

Chapter No 4. OPAMP with Feedback

OPAMP under Positive and Negative feedback, Impact Negative feedback on Bandwidth, Input and Output impedances, Offset voltage under negative feedback, Follower property & Inversion Property under linear mode operation

Chapter No 5. Linear applications of OPAMP

DC and AC Amplifier, Summing, Scaling and Averaging amplifiers (Inverting, Non-inverting and Differential configuration), Instrumentation amplifier, Integrator, Differentiator, Active Filters – First and second order Low pass & High pass filters. V to I and I to V converters.

Unit III

Chapter No 6. Nonlinear applications of OPAMP

Crossing detectors (ZCD. Comparator), Inverting Schmitt trigger circuits, Triangular/rectangular wave generators, Waveform generator, Voltage controlled Oscillator, Sample and Hold circuits, Phase Shift Oscillator, Wein Bridge Oscillator, Data Converters: Digital to Analog Converters: Weighted resistor R -2R DAC, Current steering DAC, Pipeline DAC, Analog to Digital Converters: Flash, Pipeline ADC, SAR

Text Books

- 1. Behzad Razavi, Fundamentals of Microelectronics 2nd edition, Wiley, 2013
- 2. Phillip E. Allen, Douglas R. Holberg, CMOS Analog Circuit Design 3rd edition , OUP USA, 2012
- Ramakant A. Gayakwad, Op-Amps and Linear Integrated Circuits, Pearson Education, 4th edition, 2015

Reference Books:

1. A.S. Sedra & K.C. Smith, Microelectronic Circuits, 7th edition, Oxford University Press 2017



- 2. Sergio Franco, Design with Operational Amplifiers and Analog Integrated Circuits, , 3rd edition , MHE ,2012
- 3. David A. Bell, Operational Amplifiers and Linear IC's.; Third edition, Oxford University Press, 2011
- 4. B. Razavi, Design of Analog CMOS Integrated Circuits, Second edition, McGraw Hill Education; 2017



Program: Electronics & Communication Engineering		Semester: IV
Course Title: Control Systems		Course Code: 22ECC206
L-T-P: 4-0-0	Credits: 4	Contact Hours:4 hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 50Hrs	Examination Duration: 3 Hrs	

Chapter No. 1.Control System Representation

Concepts of Control Systems- Open Loop And Closed Loop Control Systems, Feedback characteristics, Examples, System representation: Differential Equations, Transfer function, Impulse response, System modelling Electrical Mechanical, Electro mechanical, Rotational Mechanical Systems. Block Diagram Algebra and Representation by Signal Flow Graph - Reduction Using Mason's Gain Formula.

Chapter No. 2. Time Response Analysis

Standard Test Signals (impulse, step, ramp, parabola)-Order and Type of System, Time Response of First Order Systems – Characteristic Equation of Feedback Control Systems, Transient Response of Second Order Systems - Time Domain Specifications – Steady State Response - Steady State Errors and Error Constants

Chapter No. 3. Stability Analysis In S-Domain

The Concept Of Stability (BIBO, all system poles on LHS, Impulse response is convergent, Marginal stability- necessary conditions) – Routh's Stability Criterion – Limitations of Routh's Stability Criterion (Applications only).Root Locus Technique: The Root Locus Concept - Construction Of Root Loci.

Unit II

Chapter No. 4. Frequency Response Analysis

Introduction Bode Diagrams-Determination Of Frequency Domain Specifications And Transfer Function From The Bode Diagram-Phase Margin And Gain Margin-Stability Analysis From Bode Plots

Chapter No. 5. Stability Analysis In Frequency Domain

Polar Plots, Nyquist Plots Stability Analysis, Assessment Of Relative Stability Using Nyquist Criterion.

Chapter No. 6.Introduction to Controller Design

The Design Problem. Preliminary Consideration Of Classical Design, Realization Of Basic Compensators (Lag, Lead and dominant pole compensation), P, I, PI, PD & PID Controllers. **Unit III**

Chapter No. 7. State Space Analysis

State space representation of electrical systems, State Equations, STM, Eigen value and Eigen vectors, Controllability, Observability.

Text Books

- 1. J. Nagrath and M. Gopal, Control Systems Engineering; Sixth edition, New Age International Pvt Ltd 2018
- 2. B. C. Kuo, Automatic Control Systems, 9th edition, John wiley and Sons, 2014



Reference Books:

- Katsuhiko Ogata, Modern Control Engineering, 5th edition, Pearson education India Pvt. Ltd, 2015
- Richord C Dorf and Robert H. Bishop, Modern Control Systems, 13th edition, Pearson; 2016



Course Title: ARM Processor & Applications		Course Code:22EECC207
L-T-P: 3-0-0	Credits: 3	Contact Hours:3 hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 40Hrs	Examination Duration: 3 Hrs	

Chapter No. 1 ARM Architecture

The Acorn RISC machine, Architectural inheritance, Architecture of ARM7TDMI, ARM programmers model, ARM development tools, 3 stage pipeline ARM organization, ARM instruction execution.

Chapter No. 2 Introduction to ARM instruction set

Data processing instruction, Branch instruction, Load store instruction, Software interrupt instruction, Program status register instruction, Conditional execution, Example programs, introduction to thumb instruction and implementation

Chapter No. 3 Assembler rules and Directives

Introduction, structure of assembly language modules, Predefined register names, frequently used directives, Macros, Miscellaneous assembler features. Example programs.

Unit II

Chapter No. 4 Exception handling

Introduction, Interrupts, error conditions, processor exception sequence, the vector table, Exception handlers, Exception priorities, Procedures for handling exceptions.

Chapter No. 5 Introduction to Bus protocols

I2C, SPI, AMBA (advanced memory bus architecture): AHB, APB

Chapter No. 6 LPC 2148 Controller Architectural overview and GPIO programming

LPC2148 architectural overview, Registers, GPIO Programming: LED, LCD, Seven segment, Stepper Motor, DC Motor, Buzzer, Switch, Keypad.

Unit III

Chapter No. 7 On-chip programming techniques using LPC 2148 Controller

ARM interfacing techniques and programming Timers, RTC, UART, ADC, DAC, I2C and External Interrupt.

Chapter No. 8 Architectural support for high level languages

Abstraction in software design, data types, floating point data types, The ARM floating point architecture, use of memory, run time environment.

Text Books

- The 8051 Microcontroller Architecture, Programming & Applications By Kenneth. Ayala, Cenage Learning; 3^{rf} edition 2007
- 2. ARM System- on-Chip Architecture by 'Steve Furber', Second Edition, Pearson, 2015
- 3. ARM Assembly Language fundamentals and Techniques by William Hohl, CRC press CRC Press; 2nd edition,2014

Reference Books:



- 1. ARM system Developer's Guide- Hardbound, Publication date: 2004 Imprint: MORGANKAUFFMAN
- 2. User manual on LPC21XX.



Program: Electronics & Communication Engineering		Semester: IV
Course Title: Digital System Design using Verilog		Course Code: 22EECC208
L-T-P: 0-0-2	Credits: 2	Contact Hours:4 hrs/week
ISA Marks: 80	ESA Marks: 20	Total Marks: 100
Teaching Hours:	Examination Duration: 2 Hrs	
Chapter No. 1. Architecture of F	PGA	
Architecture of FPGAS: Spartan 6	5, What Is HDL, Verilog HDL Data	Types and Operators.
Chapter No. 2. Data Flow Descri	ptions	
Highlights of Data-Flow Descript	ions, Structure of Data-Flow De	scription, Data Type – Vectors,
Testbench.		
Chapter No. 3. Behavioral Descr	iptions	
Behavioral Description highlights	s, structure of HDL behavioral De	escription, The VHDL variable –
Assignment Statement, sequenti	al statements, Tasks and Functio	ons
Chapter No. 4. Structural Descriptions		
Highlights of structural Description, Organization of the structural Descriptions, state Machines,		
Generate, Generic, and Parameter statements		
Chapter No. 5:Finite State Machine:		
Moore Machines, Mealy Machines		
Chapter No. 6: Interfacing and applications		
LCD, 7 Segment display, Keyboard, Traffic light controller, Stepper Motor, DC Motor.		
Text Book		
1. Nazeih M. Botros, HDL Programming – Verilog, Dreamtech Press, 2006.		
2 I Bhaskar - A Verilog Primer: 3 rd edition Pearson Education India 2015		
References		
1. Samir Palnitkar - Verilog HDL, Pearson Education, 2 nd Edition, 2003.		
2. Thomas and Moorby -The Verilog Hardware Description Language, Kluwer academic publishers, 5 th edition, 2002.		

- 3. Stephen Brown and Zvonko Vranesic- Fundamentals of Logic Design with Verilog; 2nd edition, McGraw Hill Education 2017.
- 4. Charles. H. Roth, Jr., Lizy Kurian John Digital System Design using VHDL, Thomson, 2nd Edition, 2008.



Program: Electronics & Comm	nunication Engineering	Semester: IV	
Course Title: Data Acquisition and Control Lab		Course Code: 22EECP203	
L-T-P: 0-0-1 Credits: 1 Conta		Contact Hours: 2 hrs/week	
ISA Marks: 80	ESA Marks: 20	Total Marks: 100	
Teaching Hours:	Examination Duration: 2 Hrs		
LIST OF Experiments:	ing Tachniquae		
1. Dasic Signal Condition	ing reciniques		
a) Inverting and Nor	n Inverting Amplifier using OPAMI	D.	
b) Comparator. (ZCI) & Schmitt trigger)		
c) Precision rectifier			
2. Realize and verify th	e performance of Instrumentatio	n Amplifier using op-amp	
 Feedback Concepts: op-amp 	Realize and verify the performant	ce of Wein Bridge Oscillator using	
4. To design and imple	ment the filters for a given specif	ication	
Obtain the phase an	d frequency responses of 2nd ord	er, Low pass and High pass filter.	
5. To implement and cl	naracterize the functional block o	of ADC and DAC.	
Realize the following data converters to determine the irrespective performance parameters.			
• 4-bit R-2R DAC	• 4-bit R-2R DAC Converter.		
• 2-Bit flash ADC/	 2-Bit flash ADC/4-Bit ADC (Using 0804IC) 		
6. System Modeling			
 Realize the system modeling for DC Motor using QuanserQube 			
7. To determine System Response of RLC circuits			
Time domain response of an RLC network and the response parameters of interest			
(Rise time, Peak overshoot, Overshoot and Settling time) for critical, over and under			
damped conditions using Lab view. Time response using QuanserQube			
8. Stability Analysis			
To determine the	To determine the stability of the system depending upon Pole		
- Zero location. To	- Zero location. To determine the stability of the system using		
Bode Plots			
9. Compensation Techr	niques		
To determine suitable compensator for the given system (PD, PI, PID Controller using QuanserQube).			
10. Structured Enquiry	(16+16=32marks)		



- MOS Amplifier Design and implementation
- Design and implement a PD control system using Co-simulation.

Text Books:

- 1. Ramakant Gayakwad, Operational Amplifiers and Linear Integrated Circuits; Fourth edition Pearson Education, 2015
- 2. Sergio Franco Design with Op-amps and Analog Integrated circuits, MHE; third edition, 2012

References:

- Dan Sheingold Analog to Digital Conversion Hand Book, 3rd Revised edition PH,1986. Prentice Hall, 1985
- 2. David A. Bell, Operational Amplifiers and Linear IC's.; Third edition, Oxford University Press, 2011
- 3. Sedra and Smith Microelectronics Circuits, Sixth edition, Oxford University, 2013


Program: Electronics & Communication Engineering			Semester: IV	
Course Title: ARM Microcontroller Laboratory Experiments			Course Code: 22EECP204	
L-T-P: 0-0-1		Credits: 1	Contact Hours: 2 hrs/week	
ISA	Marks: 80	ESA Marks: 20	Total Marks: 100	
Теас	hing Hours:	Examination Duration: 2		
		Hrs		
List	of Experiments			
1	Write an ALP to achieve the followi	ng arithmetic operations:		
	i. 32 bit addition			
	ii. 64 bit addition			
	iii. Subtraction			
	iv. Multiplication			
	v. 32 bit binary divide			
	Apply suitable machine dependent	optimization technique and	l analyze for memory and time	
	consumed			
2	Write an ALD for the following usin	aloonsi		
2	write an ALP for the following using	g 100ps.		
	i. Find the sum of 'N' 16 bit n	umbers		
	ii. Find the maximum/minimu	m of N numbers		
	iii. Find the factorial of a given	number with and without l	ook up table.	
	Apply suitable machine dependent	optimization technique and	l analyze for memory and time	
	consumed			
3	Write an ALP to			
	i. Find the length of the carria	ge return terminated string	<u>.</u>	
	ii. Compare two strings for eq	uality.		
	Apply suitable machine dependent	optimization technique and	l analyze for memory and time	
	consumed			
4	Write an ALP to pass parameters to a subroutine to find the factorial of a number or prime			
	Apply suitable machine dependent optimization technique and analyze for memory and time			
	consumed			
5	Write a C program to test working o	of LEDs and seven segment	using LPC2148.	

6 Write a C program & demonstrate an interfacing of Alphanumeric LCD 2X16 panel and 4X4 keypad to LPC2148 Microcontroller.

KLE Technological University | Creating Value, Leveraging Knowledge

- 7 Write an ALP to generate the following waveforms of different frequencies
 - i. Square wave ii. Triangular iii. Sine wave
- 8 Write a program that converts the data read from sensor to a data understandable for the ARM microcontroller
- 9 Develop a C program to demonstrate the concept of serial communication with an example.
- 10 Develop an application code using embedded C to accept asynchronous inputs and control the connected device
- 11 Develop an application code using synchronous communication protocol to display the RTC value on a display device.

Text Books:

- 1. Steve Furber, ARM System- on-Chip Architecture, 2nd, LPE, 2002
- 2. The 8051 Microcontroller Architecture, Programming & Applications By Kenneth J. Ayala
- 3. Cenage Learning; 3rd edition 2007
- William Hohl ARM Assembly Language fundamentals and Techniques by, CRC press CRC Press; 2nd edition, 2014

References:

- 1. ARM system Developer's Guide- Hardbound, Publication date: 2004Imprint: MORGANKAUFFMAN
- 2. User manual onLPC21XX.



Program: Electronics & Commur	Semester: IV	
Course Title: Data Structures Ap	Course Code: 21EECF201	
L-T-P: 0-0-2	Credits: 2	Contact Hours: 4 hrs/week
ISA Marks: 80 ESA Marks: 20		Total Marks: 100
Teaching Hours: Examination Duration: 2		

Chapter No 1. Analysis of algorithms: Introduction, Asymptotic notations and analysis, Analysis of recursive and non-recursive algorithms, master's theorem, complexity analysis of algorithms. **Chapter No 2.** Analysis of linear data-structures and its applications: Complexity analysis of basic data structures (Stacks, Queues, Linked lists)

Unit II

Chapter No 3. Analysis of non-linear data-structures and its applications

Trees and applications: Computer representation, Tree properties, Binary Tree properties, Binary search trees properties and implementation, Tree traversals, AVL tree.

Graphs and applications: Computer representation, Adjacency List, Adjacency Matrix, Graph properties, Graph traversals. Hashing and applications: Hashing, Hash function, Hash Table, Collision resolution techniques, Hashing Applications

Text Books

- 1. Richard F. Gilberg & Behrouz A. Forouzan, Data Structures A Pseudocode Approach with C, Second Edition.
- 2. Aaron M. Tenenbaum, Data Structures Using C.



Program: Electronics & Communication Engineering Se				Semester: IV
Course Ti	tle: Data Structures using C	Diploma) Co		Course Code: 21EECF203
L-T-P: 0-0	-3	Credits: 3 Co		Contact Hours: 6 hrs/week
ISA Mark	s: 80	ESA Marks: 20		Total Marks: 100
Teaching	Hours:	Examination D 2 Hrs	uration:	
	List of experiments/jobs planned to meet the requireme			nents of the course.
Category	y: Demonstration	Total Weightage	: 0.00	No. of lab sessions: 6.00
Expt./	Experiment / Job Details	No. of Lab	Marks /	Correlation of Experiment
Job No.		Session(s) per	Experime	nt with the theory
		batch		
		(estimate)		
1	Drograme on Deinter	2.00	0.00	
	Programs on Pointer	2.00	0.00	
	concepts.			
	Learning Objectives :			1
	The students should be able	e to		
	Perform basic programming	g structures on		
	1. Pointers concepts.			
	2. 1D and 2Darrays.			
	3. Pointers to functions.			
	4. Memory management fu	nctions		
2	Programs on string	2.00	0.00	
	handling functions,			
	structures union And bit-			
	files.			
	Learning Outcomes			1
	The students should be able	to write program	ns to:	1
	a)Dorform string bondling fu	unationa lika	15 10.	
	a)Perform string handling h	unctions like		
	1. String length.			
	2. String concatenate.			
	3. Strings compare.			
	4. String copy.			



	5. Strings reverse. b) Implement Structures, union and bit-field			
3	Programming on files.	2.00	0.00	
	Learning Outcomes: The students should be able to write a modular program to:			1
	1. Open and Close the file.			
	2. Read and Write the file.			
	3. Append the file.			
Category	y: Exercise	Total Weightage	: 20.00	No. of lab sessions: 12.00
Expt./ Job No.	Experiment / Job Details	No. of Lab Session(s) per batch (estimate)	Marks / Experiment	Correlation of Experiment with the theory
4	Programs on implementation of stacks and its applications.	2.00	3.00	
5	Learning Outcomes: The students should be able 1. Write a program to Inser elements for an application 2. Write a program using sta postfix & Infix to Prefix 3. Write a program using sta conversion. Programs on implementation of different queue data structures.	nes: build be able to: am to Insert delete and display stack application. am using stack to convert from Infix to Prefix am using stack data structure for base 2.00 4.00		3
	Learning Outcomes: The students should be able to:			3



	Write a program using queue data structure for an application.			
6	Programs on implementation of different types of Linked lists	2.00	4.00	
	Learning Outcomes: The students should be able to write a modular program to use the linked lists for an application 1. Insert, delete and display a node in SLL. 2. Insert, delete and display a node in DLL.			4
	3. Insert delete and display	a node in CLL.		
7	Programs on Implementation of trees.	2.00	3.00	
	Learning Outcomes: The students should be able to :	e to write modular	r programs	5
	1. Perform various operatio	ons on binary trees	s.	
	2. To find max, min value in	a binary search t	rees.	
	3. To find the height of a tre	ee,		
	4. To count nodes in a tree.			
	5. To delete a node in a tree	9		
8	Programs to implement different sorting techniques.	2.00	3.00	
	Learning Outcomes: The students should be able to: Write modular program on perform the following sorting techniques 1. Selection			5

KLE Technological University Creating Value, Leveraging Knowledge

	2. Insertion3. Bubble					
	4. Merge					
	5. Quick					
	6. Неар					
9	Programming on hash tables	2.00	3.00			
	Learning Outcomes: The students should be able to Write modular program on			6		
	 Direct-address table Hash tables 	S				
Books/R	eferences:					
1.	Aaron M. Tenenbaum, et al	, "Data Structures	s using C", PHI	, 2006		
2.	2. Cormen, Leiserson, Rivest "Introduction to Algorithms", PHI, 2001					
3.	3. E Balaguruswamy, "The ANSI C programming Language", 2ed, PHI, 2010.					
4.	4. Yashavant Kanetkar, "Data Structures through C", BPB publ			lications 2010		
5.	 Horowitz, Sahani, Anderson-Feed, "Fundamentals of Data Structures in C' 2ed, Universities Press, 2008 			C",		
6.	 Richard F. Gilberg, Behrouz A. Forouzan "Data Structures: A Pseudocode Approach with C", 2nd Edition, Course Technology, Oct 2009. 					

7. Kernighan and Ritchie, The ANSI C programming Language, 2 ed., PHI. Robert Kruse,

Data Structures and Program Design in C, 2 ed., Pearson



Program: Electronics & Commun	Semester: V	
Course Title: CMOS VLSI Circuits	Course Code: 19EECC301	
L-T-P: 4-0-0 Credits: 4		Contact Hours:4 hrs/week
ISA Marks: 50 ESA Marks: 50		Total Marks: 100
Teaching Hours: 50Hrs		

Chapter No. 1. Introduction to VLSI and IC fabrication technology

VLSI Design Flow, Semiconductor Technology - An Overview, Czochralski method of growing Silicon, Introduction to Unit Processes (Oxidation, Diffusion, Deposition, Ion-implantation), Basic CMOS technology - Silicon gate process, n-Well process, p-Well process, Twin-tub Process, Oxide isolation. FinFET device, The root cause of short channel effects in twenty-first century MOSFETS, The thin body MOSFET concept, The FinFET and a new scaling path for MOSFETs, Ultra-thin body FET, Recent trends in fabrication technology.

Chapter No. 2. Electronic Analysis of CMOS logic gates

DC transfer characteristics of CMOS inverter, Beta Ratio Effects, Noise Margin, MOS capacitance models. Transient Analysis of CMOS Inverter, NAND, NOR and Complex Logic Gates, Gate Design for Transient Performance, Switch-level RC Delay Models, Delay Estimation, Elmore Delay Model, Power Dissipation of CMOS Inverter, Transmission Gates & Pass Transistors, Tristate Inverter. **Unit II**

Chapter No. 3. Design of CMOS logic gates

Stick Diagrams, Euler Path, Layout design rules, DRC, Circuit extraction, Latch up – Triggering Prevention.

Chapter No. 4. Designing Combinational Logic Networks

Gate Delays, Driving Large Capacitive Loads, Delay Minimization in an Inverter Cascade, Logical effort. Pseudo nMOS, Clocked CMOS, Dynamic CMOS Logic Circuits, Dual-rail Logic Networks: CVSL, CPL.

Unit III

Chapter No. 5. Sequential CMOS Circuit Design

Sequencing static circuits, Circuit design of latches and flip-flops, Clocking- clock generation, clock distribution.

Text Books

- 1. John P. Uyemura, Introduction to VLSI Circuits and Systems, 1, Wiley, 2007
- 2. Neil Weste, David Harris & Ayan Banerjee, CMOS VLSI Design, 4, Pearson Ed 2011
- 3. Sung-Mo Kang & Yusuf Leblebici, CMOS Digital Integrated Circuits: Analysis and Design, Tata McGra, 2007

Reference Books:

- FinFET Modeling for IC Simulation and Design: Using the BSIM-CMG Standard By Yogesh Singh Chauhan, Darsen Duane Lu, Vanugopalan Sriramkumar, Sourabh Khandelwal, Juan Pablo Duarte, Navid Payvadosi, Ai Niknejad, Chenming Hu, Elsevier Publication, 2015
- 2. Wayne, Wolf, Modern VLSI design: System on Silicon, 3, Pearson Ed, 2005
- 3. Douglas A Pucknell and Kamran Eshraghian, Basic VLSI Design, 3rd edition, PHI, 2005
- 4. Phillip. E. Allen, Douglas R. Holberg, CMOS Analog circuit Design, 3rd edition, Oxford University, 2011





Program: Electronics & Commun	Semester: V			
Course Title: Communication Sy	Course Code: 23EECC302			
L-T-P: 3-0-1 Credits: 4		Contact Hours:5 hrs/week		
ISA Marks: 50 ESA Marks: 50		Total Marks: 100		
Teaching Hours: 40Hrs Examination Duration: 3 Hrs				

Chapter 01. Introduction to Analog communication

Introduction, history of communication, need for modulation, Amplitude modulation, Time-Domain and Frequency domain description, Frequency-Domain description, DSBSC, SSB, VSB, Phase and frequency modulation, Phase and frequency Deviation, Narrow and Wide band frequency modulation. Spectrum and phase diagram of FM Transmission band width of FM waves, Effect of Modulation index on bandwidth, Comparison of all modulation techniques.

Chapter 02. Sampling Process

Sampling theorem, Quadrature sampling of Band pass signals, Reconstruction of a message from its samples. Time Division Multiplexing (TDM) Signal distortion in Sampling. Pulse Amplitude Modulation (PAM), Pulse Position Modulation (PPM), Pulse Width Modulation (PWM)

Unit II

Chapter 03. Waveform Coding Techniques

Pulse-Code Modulation, Channel noise and Error Probability, Quantization noise and Signal to noise ratio, Robust Quantization, Differential Pulse code modulation, Delta Modulation, Problems

Chapter 04. Baseband shaping for data transmission

Discrete PAM signals, Power spectra of discrete PAM signals, Intersymbol Interference, Nyquist'scriterion for distortionless baseband binary transmission, correlative coding, eye pattern, baseband M-ary PAM systems, and adaptive equalization for data transmission, Problems

Unit III

Chapter 05. Digital Modulation Techniques

Digital Modulation formats, Coherent binary modulation techniques, Coherent quadrature modulation techniques, Non-coherent binary modulation techniques, Comparison of Binary and Quaternary Modulation techniques, Problems

Text Books

- 1. "Communication Systems" by 'Simon Haykin' John Wiley 2003. 5th edition , 2009
- 2. "Principles of communication Systems", by Taub & Schilling, 2nd edition, TMH.
- 3. "Digital communications", Simon Haykin, John Wiley, 2006

Reference Books:

- 1. Communication Systems, by B.P.Lathi,
- 2. Ganesh Rao, K N Haribhat, Analog Communication, Sanguine, 2009
- 3. Communication Systems by Harold. P.E, Stern Samy. A. Mahmond, Pearson Education, 2004.
- 4. Electronic communication systems, Kennedy and Davis, TMH, Edn. 6, 2012



Back to Semester V

Program: Electronics & Commun	Semester: V	
Course Title: Digital Signal Proce	Course Code: 23EECC303	
L-T-P: 2-0-2 Credits: 4		Contact Hours:6 hrs/week
ISA Marks: 80	ESA Marks: 20	Total Marks: 100
Teaching Hours: 30Hrs Examination Duration: 3 Hrs		

Unit I

Discrete Fourier Transforms

Brief review of signals and systems: Basic definitions, properties and applications. Discrete Fourier Transforms (DFT), DFT as a linear transformation, Properties of DFT, Use of DFT in linear filtering, Overlap-save and Overlap-add method.

Unit II

Fast-Fourier-Transform (FFT) algorithms Fast-Fourier-Transform (FFT) algorithms: Direct computation of DFT, Need for efficient computation of the DFT (i.e. FFT algorithms), Radix-2 FFT algorithm for the computation of DFT and IDFT: Decimation-in-time and Decimation-in-frequency algorithms.

Unit III

Design of digital IIR and FIR filters Design of IIR filters: Butterworth and Chebyshev methods using impulse invariance technique, and bilinear transformation. Design of linear phase FIR filters using windowing method - Rectangular, Hamming, Hanning, Bartlet and Kaiser windows.

Text Books

- 1. Proakis & Manolakis, Digital signal processing Principles Algorithms & Applications, 4th edition, PHI, New Delhi, 2007
- 2. S.K. Mitra, Digital Signal Processing, 2nd edition, Tata Mc-Graw Hill, 2004

Reference Books:

1. Oppenheim & Schaffer, Discrete Time Signal Processing, 5th edition, PHI, New Delhi, 2000



Program: Electronics & Commun	Semester: V	
Course Title: Operating System a	Course Code: 22EECC304	
L-T-P: 3-0-0 Credits: 3		Contact Hours: 3 hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 40Hrs Examination Duration: 3 Hrs		

Chapter 1: Introduction and System structures

What is an operating system? Goals of an operating system. Operation of an OS .Resource allocation and related functions. Classes of an operating system. Operating System Services. System Calls and Types. Operating system Structure – Simple, Layered, Microkernels, Modules and Hybrid systems. System Boot

Chapter 2: Process Management

Process concept- operating on process, inter process communication, process scheduling- CPU scheduler- pre-emptive scheduling , scheduling criteria, scheduling algorithms- first come first served scheduling, shortest job first scheduling, priority scheduling, round robin scheduling.

Chapter 3: Memory Management

Memory Management Strategies: process address space static vs dynamic loading. Swapping, memory allocation; fragmentation Paging; Structure of page table; Segmentation, Virtual Memory.

Unit II

Chapter 4: Introduction To Real-Time Operating Systems

Introduction To Real-Time Operating Systems: Introduction to OS, Introduction to real time embedded system- real time systems, characteristics of real time systems and the future of embedded systems. Introduction to RTOS, key characteristics of RTOS, its kernel, components in RTOS kernel, objects, scheduler, services, context switch, Scheduling types: Pre-emptive priority-based scheduling, Round-robin and pre-emptive scheduling.

Chapter 5: Tasks, Semaphores and Message Queues

Tasks, Semaphores and Message Queues: A task, its structure, A typical finite state machine, Steps showing the how FSM works. A semaphore, its structure, binary semaphore, mutual exclusion (mutex) semaphore, Synchronization between two tasks and multiple tasks, Single shared-resource-access synchronization, Recursive shared- resource-access synchronization. A message queue, its structure, Message copying and memory use for sending and receiving messages, Sending messages in FIFO or LIFO order, broadcasting messages.

Unit III

Chapter 6: Typical Embedded System and bus protocols

Classification and purposes of embedded system, Characters and Quality attributes of embedded system, Core and Supporting components of embedded system, Embedded firmware, AMBA Bus Protocol, SPI, RS 485, wireless protocols (Bluetooth, 802.11 and its variants, ZigBee)

Chapter 7: Case study

Applications based on Cortex M series in RTOS environment

Reference Books:



1. Dhananjay Dhamdhere, Operating Systems a Concept Based Approach, 3rd edition, McGraw-HillEducation, 2017



Program: Electronics & Commun	Semester: V	
Course Title: Machine Learning	Course Code: 23EECC307	
L-T-P: 2-0-1 Credits: 3		Contact Hours:4 hrs/week
ISA Marks: 50 ESA Marks: 50		Total Marks: 100
Teaching Hours: 30Hrs Examination Duration: 3 Hrs		

Chapter No.1 Introduction

Motivation, History and Evolution, Definition (ETP, Examples), Types of Machine Learning: Supervised, Unsupervised and Reinforcement learning.

Chapter No. 2 Supervised Learning

Model Representation: Basic Terminologies (Variable/features, Input, Output, Model, Learning Algorithm, Hypothesis, Cost/Loss function) Linear Regression: Single Variable (Representation of hypothesis, cost function, Optimization: Sum of squared error (L1 and L2), parameters/weights, bias) without bias and with bias. Model Optimization: Introducing Iterative optimization (Sum of squares error function, Gradient descent algorithm) and non-iterative optimization. Linear Regression: Polynomial Regression and Multi-variable Regression (Representation of hypothesis, cost function, Optimization).Model Optimization: Gradient descent algorithm (Learning rate/ step size, Normalization/ Feature Scaling).Model Optimization: Non-iterative optimization (Normal Equation).Logistic Regression: Hypothesis Representation, Decision boundary, Cost function, Logistic Regression: Optimization (Gradient Descent), Multi-class classification (One-vs.-all classification using logistic regression), Classical supervised learning algorithm- Support Vector Machine (SVM)

Chapter No. 3 Performance Evaluation

Performance Evaluation of learning models: Metrics (Confusion matrix, Precision, Recall, F1 Score, RoC curves), modelling data and validating learning, Over fitting, Trade of Bias and Variance, Methods to overcome over fitting (Feature reduction, Regularization)

Unit II

Chapter No. 4 Unsupervised Learning Clustering

Introduction, K-means Clustering, Algorithm, Cost function, Applications, Dimensionality Reduction: Motivation, Definition, Methods of Dimensionality reduction, Dimensionality Reduction: PCA- Principal Component Analysis

Chapter No. 5 Introduction to Neural Network and deep learning

Introduction to Neural Networks (Motivation: non-linear model, Neurons and perception), Model representation: Neural Network Architecture (Activation units, Layers), Neural Network: Initialization, Forwards propagation, and Cost function, Back propagation algorithm, Multi-class classification, Steps to train a neural network, Applications of Neural Networks, Introduction to Deep Learning (Motivation, Overview), Convolution Neural Networks (CNN) (Architecture, terminologies, Evolution and Modelling)

Unit III

Chapter No. 6 Deep learning algorithms

Recurrent Neural Networks (RNN), Self-supervised models (Auto encoders and variants), Generative Models (GAN, its variants and applications)

KLE Technological University Creating Value, Leveraging Knowledge

Chapter No. 7 Sequence to Sequence Learning

Attention networks, Transformer based architecture, Transformer for Time-Series

Text Books

- 1. Tom Mitchell, Machine Learning, 1, McGraw-Hill, 1997
- 2. Christopher Bishop, Pattern Recognition and Machine Learning, 1, Springer, 2007

Reference Books:

1. Trevor Hastie, Robert Tibshirani, Jerome Friedman, The Elements of Statistical Learning : Data Mining Inference and Prediction, 2, Springer, 2009



Program: Electronics & Commu	Semester: V			
Course Title: CMOS VLSI Circuit	Course Code: 19EECP301			
L-T-P: 0-0-1 Credits: 1		Contact Hours: 28Hrs		
ISA Marks: 80	ESA Marks: 20	Total Marks: 100		
Teaching Hours:				
List of Experiments:				

- 1. Introduction to Cadence EDA tool.
- 2. Static and Dynamic Characteristic of CMOS inverter.
- 3. Layout of CMOS Inverter(DRC,LVS)
- 4. Static and Dynamic Characteristic of CMOS NAND2 and NOR2.
- 5. Layout of NAND2, NOR2, and XOR2 gates (DRC, LVS).

Structured Enquiry

1. Design a Phase Detector using D-FF

Open Ended

1. Design complex combinational circuits and analyse the performance using Cadence tool.

Books/References:

- 1. John P. Uyemura, -Introduction to VLSI Circuits and Systems, Wiley, 2006.
- 2. Neil Weste and K. Eshragian, Principles of CMOS VLSI Design: A System Perspective,2nd edition, Pearson Education (Asia) Ptv. Ltd., 2000.



Program: Electronics & Communication Engineering		Semester: V		
Course Title: RTOS Lab		Course Code: 22EECP302		
L-T-P: 0-0-1 Cre		Credits: 1	Contact Hours: 2 hrs/week	
ISA N	1arks: 80	ESA Marks: 20	Total Marks: 100	
Teach	ning Hours:	Examination Duration: 2 Hrs		
1	Develop 'C' program & demonstra performance.	ate basic Scheduling algorithms	s using Cortex M3 and comment on	
2	Write an optimized 'C' program comment on performance.	to demonstrate the concept of	f semaphore using Cortex M3 and	
3	Write an optimized 'C' program comment on performance.	a & demonstrate concept of R	Round Robin Task Scheduling and	
4	Write an optimized 'C' progran algorithm by using RTX Kernel and	n to demonstrate the concep d comment on performance.	t of basic preemptive scheduling	
5	Write an optimized 'C' program & demonstrate concept of Events and Flags for inter task communication using RTX Kernel. Also comment on performance.			
6	Write an optimized 'C' program & demonstrate concept of Mailbox and comment on performance.			
7	Write an optimized 'C' program & demonstrate concept of Semaphore and comment on performance.			
8	Write an optimized 'C' program & demonstrate concept of interrupts (hardware and software). Also comment on performance.			
9	Write an optimized 'C' program to interface I2C-RTC with LPC2148 and comment on performance.			
10	Write an optimized 'C' program to interface SPI-EEPROM with LPC2148 and comment on performance.			
Book	s/References:			
1	1. ARM System- on-Chip Architecture by 'Steve Furber, LPE, Second Edition, Addison Wesley; 2000.			
2	. Embedded Systems - Arcl edition, TMH, 2017	nitecture, Programming a	nd Design by Raj Kamal, 3 rd	
3	 Dr.K.V.K.K.Prasad—Embede published by dreamtech pr 	ded/Realtime systems: con ess, 2003.	cepts, Design & Programming,	
Manual				
1.	LPC2148 datasheet by NXP			

2. LPC2148 board manual by ALS, Bangalore.



Program: Electronics & Communication Engineering			Semester: \	/		
Course Title: Mini Project			Course Cod	e: 23EECW301		
L-T-P: 0-0-3 Cre		Credits: 3	3		Contact Ho	urs: 6 hrs/week
ISA Marks: 50		ESA Mar	ks: 50		Total Marks	: 100
Teaching Hours: 2	8	Examinat	tion Du	ration: 2 Hrs		
Guide lines for sel	ection of a pro	oject:				
1. The projec	t needs to en	compass	the cor	ncepts leant in	i a subject/s	studied in the
previous fo	our semesters,	so that th	e stude	ent will learn to	integrate, th	ne knowledge base
acquired to	o provide a sol	ution to th	ne ider	tified need.		
2. Project sho	ould be able to	exhibit se	nsing, c	controlling and	actuation se	ctions.
3. The mini p	roject essentia	lly will cor	nprise o	of two compon	ents:	
The hai	rdware design					
• The gra	aphical user in	nterface (GUI) fo	or application	and data an	alysis with report
genera	tion.					
Г			1 1			1
	Data acqu	isition		Program	imable	
	and Droop	ooina		oontrollor		
Input —		ssing		CONTIONERS	s (µp,µc,	→ Output
	(Analog,Dig	ital,LIC,		FPGA,CPL	D,Assembl	
				y/Highleve	ghlevel /HDL)	
	5&5, D	5P)]
		Con	itrol Sy	rstem		
4. Student ca	n select a proi	ect. which	leads	to a product or	model or pr	ototype related to
following a	reas (not limit	ed to thes	e areas).	inclusion pr	

- Pulse and digital circuits: simulate the working of one or more circuits
- Signals and systems: simulate the behaviour of a system by considering different signals
- Analog Electronic: simulate working of different devices
- Control systems: simulate the behaviour of a control system
- Linear Integrated Circuits: simulate working of one or more circuits
- Micro-controllers: simulate the ALU/control unit of microcontroller
- 5. Time plan: Effort to do the project should be between 120-150 Hrs per team, which includes self-study of an individual member (80-100 Hrs) and teamwork (40-50hrs).
- 6. Learning overhead should be 20-25% of total project development time.



Back to Semester V

Progra	Program: Electronics & Communication Engineering		Semester: V
Course Title: Arithmetical Thinking and Analytical Reasoning		Course Code: 23EHSA303	
L-T-P: (0-0-0	Credits: 0	Contact Hours: 1 hrs/week
ISA Ma	arks: 50	ESA Marks: 50	Total Marks: 100
Teachi	ng Hours: 16Hrs	Examination Duration: 3 Hrs	
Chapt	er No. 1. Analytical Thinki	ng	
Import	ance of Sense of Analysi	s for Engineers, Corporate Me	thodology of Testing Sense of
Analys	is, Puzzles for practice: A	Analytical, Mathematical, Classi	fication Puzzles, Teamwork in
Proble	m Solving		
Chapt	er No. 2. Mathematical Th	ninking I	
Problems on Finance: Percentages, Gain and Loss, Interest; Distribution and Efficiency Problems:			
Averag	ges, Time Work, Permutation	ons Combinations	
Chapter No. 3. Mathematical Thinking II			
Distribution Problems: Permutations Combinations			
Chapt	er No. 4. Verbal Ability		
Compr	ehension of Passages, Err	or Detection and Correction Exe	ercises, Common Verbal Ability
questi	questions from Corporate Recruitment Tests		
Refere	nce Books:		
1.	1. George J Summers, "The Great Book of Puzzles & Teasers", Jaico Publishing House, 1989		
2.	Shakuntala Devi, "Puzzles to Puzzle You", Orient Paper Backs, New Delhi, 1976		
3.	R. S. Aggarwal, "A Modern Approach to Logical Reasoning", Sultan Chand and Sons, New		
	Delhi, 2018		
4.	M Tyra, "Magical Book or	Quicker Maths", BSC Publicatio	ns, 2018
5.	Cambridge Advanced Lea	rner's Dictionary, Cambridge Un	iversity Press.
6.	Kaplan's GRE guide		



Program: Electronics & Commur	Semester: VI			
Course Title: Professional Aptitu	Course Code: 23EHSA302			
L-T-P: 0-0-0	Credits: Audit	Contact Hours:4 hrs/week		
ISA Marks: 50	ESA Marks: 50	Total Marks: 100		
Teaching Hours: 40Hrs	Examination Duration: 3 Hrs			
Unit I Chapter 1. – Arithmetical Reasoning Chapter 2. – Analytical Thinking Chapter 3. – Syllogistic Logic				
Unit II				
Chapter 1. – Verbal Logic				
Chapter 2. – Non-Verbal Logic				
Unit III				
Chapter 1 Lateral Thinking				
Text Books				
 A Modern Approach to Verbal and Non – Verbal Reasoning – R. S. Aggarwal, Sultan Chand and Sons, New Delhi 				
2. Quantitative Aptitude – R. S. Aggarwal, Sultan Chand and Sons, New Delhi				
Reference Books:				
 Verbal and Non – Verbal Reasoning – Dr. Ravi Chopra, MacMillan India 				

2. Lateral Thinking – Dr. Edward De Bono, Penguin Books, New Delhi

KLE Technological University Creating Value, Leveraging Knowledge

Program: Electronics & Commun	Semester: VI	
Course Title: Industry Readiness & Leadership Skills		Course Code: 23EHSA304
L-T-P: 0-0-0	Credits: 0	Contact Hours: 1 hrs/week
ISA Marks: 25	ESA Marks: 75	Total Marks: 100
Teaching Hours: 16Hrs	Examination Duration: 3 Hrs	

Chapter No. 1. Written Communication

Successful Job Applications, Résumé Writing, Emails, Letters, Business Communication, Essay, and Paragraph Writing for Recruitment Tests

Chapter No. 2. Interview Handling Skills

Understanding Interviewer Psychology, Common Questions in HR Interviews, Grooming, Interview Etiquette

Chapter No. 3. Lateral & Creative Thinking

Lateral Thinking by Edward de Bono, Fractionation and Brain Storming, Mind Maps, Creativity Enhancement through Activities

Chapter No. 4. Team Building & Leadership Skills

Communication in a Team, Leadership Styles, Playing a Team member, Belbin's team roles, Ethics, Effective Leadership Strategies

Reference Books:

- 1. Diana Booher E Writing, Laxmi Publications
- 2. Edward de Bono-Lateral Thinking A Textbook of Creativity, Penguin UK
- 3. William Strunk, E B White The Elements of Style, Pearson
- 4. John Maxwell The 17 Essential Qualities of a Team Player, HarperCollins Leadership
- 5. Robin Ryan 60 Seconds and You're Hired! Penguin Books



Program: Electronics & Commur	Semester: VI		
Course Title: Automotive Electro	Course Code: 22EECC305		
L-T-P: 3-0-0	Credits: 3	Contact Hours: 3 hrs/week	
ISA Marks: 50	ESA Marks: 50	Total Marks: 100	
Teaching Hours: 40Hrs Examination Duration: 3 Hrs			

Chapter No: 1. Introduction to Vehicle Drivelines / Power train Systems

Overview of Automotive industry, ECU Design Cycle: Types of model development cycles (V and Agile), Components of ECU, Examples of ECU on Chassis, Infotainment, Body Electronics and cluster. Introduction to power train, manual and automatic transmissions, automotive axles, 4-wheel and 2-wheel drives, Vehicle braking fundamentals, Steering Control, Overview of Hybrid Vehicles,

Chapter No: 2. Automotive Control Systems Design

Derivation of models and design of control strategies for power train control modules and integration into automotive platforms. Engine control functions, Fuel control, Electronic systems in Engines, Development of control algorithm for EMS with consideration of vehicle performance. Automotive grade microcontrollers: Architectural attributes relevant to automotive applications, Automotive grade processors ex: Renesas, Quorivva, and Infineon.

Chapter No: 3. Automotive Sensors and Actuators

Sensor characteristics, Sensor response, Sensor error, Redundancy of sensors in ECUs, Avoiding redundancy, Smart Nodes, Examples of sensors: Accelerometer (knock sensors), wheel speed sensors, Engine speed sensor, Vehicle speed sensor, Throttle position sensor, Temperature sensor, Mass air flow (MAF) rate sensor, Exhaust gas oxygen concentration sensor, Throttle plate angular position sensor, Crankshaft angular position/RPM sensor, Manifold Absolute Pressure (MAP) sensor. Actuators: Engine Control Actuators, Solenoid actuator, Exhaust Gas Recirculation Actuator.

Unit II

Chapter No: 4. Automotive Stability and Safety Systems

Passive/active safety systems and design philosophies. Investigation of stability issues associated with vehicle performance and the use of sensors and control system strategies for stability enhancement. Implementation and application to intelligent cruise control, lane departure warning systems, ABS, Traction Control, active steering systems, vehicle dynamic control systems.

Chapter No: 5. Automotive communication protocols

Overview of Automotive communication protocols : CAN, CAN FD, SOME/ IP Protocol, LIN , Flex Ray, MOST

Unit III

Chapter No: 6. Overview of ADAS/AV and Functional safety standards

Advanced Driver Assistance Systems (ADAS), Autonomous vehicle basics, sensing, planning and controls for autonomous driving, connected vehicles.

Functional Safety: Need for safety standard-ISO 26262, safety concept, safety process for product life cycle, safety by design, validation.

Chapter No: 7. Diagnostics and Reliability

Discussion of legislated state, federal and international requirements. On-board automotive sensors to monitor vehicle operation, typical diagnostic algorithms. Analytical methods for designing fault-tolerant systems and assessing vehicle reliability, including safety critical systems



and 'limp-home' modes. Use of handheld scanners and specialized diagnostic equipment to classify faults. Diagnostic protocols: KWP2000 and UDS.

Text Books

- 1. Ribbens, Understanding of Automotive electronics, 8th edition , Elsevier, 2017
- 2. Denton. T, Automobile Electrical and Electronic Systems, 5th edition, Routledge, 2017
- 3. Denton. T , Advanced automotive fault diagnosis, 4th edition Routledge, 2016

Reference Books:

- 1. Ronald K Jurgen, Automotive Electronics Handbook, 2nd Edition, McGraw-Hill, 1999
- 2. James D Halderman, Automotive electricity and Electronics, 5th edition, Pearson, 2016
- 3. Allan Bonnick, Automotive Computer Controlled Systems Diagnostic Tools and Techniques, Elsevier Science, 2001
- 4. Nicholas Navet , Automotive Embedded System Handbook , 2009



Program: Electronics & Commun	Semester: VI		
Course Title: Computer Communication Networks I		Course Code: 23EECC306	
L-T-P: 4-0-0	Credits: 4	Contact Hours: 4 hrs/week	
ISA Marks: 50	ESA Marks: 50	Total Marks: 100	
Teaching Hours: 50Hrs			

Chapter No.1. Computer Networks and the Internet

What is Internet? The Network Edge, the network Core, delay-loss, throughput in packet switched networks. Protocol layers(OSI layers) and their service models, networks under attack

Chapter No. 2. Application Layer

Principles of network applications, the web and HTTP,DHCP, electronic mail in the internet, DNS, peer-to-peer applications

Unit II

Chapter No. 3. Transport Layer

Introduction and transport-layer services-relationship between transport and network layers - overview of the transport layer in the internet, multiplexing and de multiplexing, connectionless transport: UDP, principles of reliable data transfer, connection oriented transport TCP, TCP congestion control.

Chapter No. 4. Network layer

Introduction, virtual circuit and datagram networks, what's inside router? The Internet protocol (IP): forwarding and addressing in the internet.

Unit III

Chapter No. 5. Network layer

Routing algorithms: Link-State (LS), Distance-Vector (DV), Hierarchical Routing, Routing in the Internet, Intra-AS routing RIP, OSPF, Inter-AS routing BGP, broadcast routing algorithms and multi cast routing

Text Books

1. Kurose & Ross, Computer Networking A Top-Down Approach, 6th edition, PEARSON, 2013. **Reference Books:**

1. Behrouz A. Forouzan, 1. Data Communications and Networking , 4th Edition, Tata McGraw, 2006

2. Larry L. Peterson and Bruce S. Davie, Computer Networks A Systems Approach, : 4th Edition, Elsevier



Program: Electronics & Communication Engineering		Semester: VI
Course Title: Computer Communication Networks I Lab		Course Code: 23EECP303
L-T-P: 0-0-1	Credits: 1	Contact Hours: 2 hrs/week
ISA Marks: 80	ESA Marks: 20	Total Marks: 100
Teaching Hours:	Examination Duration: 2 Hrs	
Experiment wise plan		
1. Implement echo server using	socket.	
2. Implement a chat application	using multiple client sockets.	
3. Write a program to transfer a	file from server using sockets.	
4. Write a program for impleme	nt Cyclic Redundancy Check	
5. Introduction to network oper	ating system	
6. Configure and demonstrate a VLAN.		
7. Configure and analyze OSPF		
8. Configure and demonstrate DHCP		
OPEN ENDED:		
9. Configure and analyze BGP		
OR		
10. Implement a Socket applicat	ion	
Text Books:		
1. Kurose & Ross, Computer	Networking A Top-Down Appro	ach, 6 th edition PEARSON, 2013.
Reference Books:		
1. Cisco networking academ	y, https://www.netacad.com/	
2. Juniper networking acade	emy, https://learningportal.juni	per.net/



Program: Electronics & Communication Engineering		Semester: VI	
Course Title: Automotive Electro		onics Lab	Course Code: 22EECP304
L-T-P: 0-0-1		Credits: 1	Contact Hours: 2 hrs/week
ISA Marks: 80		ESA Marks: 20	Total Marks: 100
Teachin	ng Hours:	Examination Duration: 2 Hrs	
1	Demonstration of cut section modules: Engine, Transmission, Steering, Braking, Suspension		
2	Simulink Onramp		
3	Modeling a vehicle motion acceleration.	on a flat surface during hard acc	eleration, deceleration and steady
4	Automotive suspension mod	leling using simulink and simscape	
5	EGAS modeling and simulation using Simulink and realization on the hardware platform.		
6	Realization of vehicle speed control based on the gear input on hardware platform.		
7	Interior lighting control and seat belt warning system modeling with state flow and realization on the hardware platform.		
8	Modeling and simulation of Automatic temperature Control using stateflow and simulink.		
8	Gear input transmission over CAN bus using ARM Cortex m3 and signal analysis using CANalyzer/BusMaster software.		
9	Realize Steer by wire system using model based design		
10	Design and develop advance driver assistance system using simulink and realization on the hardware platform.		
Text Bo 1.	oks Ribbens, Understanding c	of Automotive electronics, 6 th , E	lsevier, 2003

2. Denton.T, Automobile Electrical and Electronic Systems, 5th edition, Routledge, 2017



Program: Electronics & Commun	Semester: VI	
Course Title: Minor Project I	Course Code: 23EECW302	
L-T-P: 1-0-4	Credits: 5	Contact Hours: 9 hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 14Hrs		

Program: Electronics & Commun	Semester: VI	
Course Title: Minor Project II	Course Code: 23EECW303	
L-T-P: 0-0-5	Credits: 5	Contact Hours: 10 hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 14Hrs		

Application Areas are,

- Smart City
- Connected Cars
- Home Automation
- Health care
- Smart energy
- Agriculture

Guide lines for selection of a project:

1. The project needs to encompass the concepts leant in a subject/s studied in the previous five semesters, so that the student will learn to integrate, the knowledge base acquired to provide a solution to the defined problem statement of the minor-projects.

2. Student can select a project, which leads to a product or model or prototype.

3. Time plan: Effort to do the project should be between 120-150 Hrs per team, which includes self-study of an individual member (80-100 Hrs) and teamwork (40-50hrs).

4. Learning overhead should be 20-25% of total project development time.

Criteria for group formation :

- 1. 3-4 students in a team.
- 2. Role of teammates: Team lead and members.

Allocation of Guides and Mentors for the projects: Every Project batch will be allocated with one faculty. Details of the project batches:

1. Number of faculty members : 64

2. Number of students: 278

Role of a Guide

The primary responsibility of the guide is to help students to understand the meaning and need of various stages in the implementation of the project. At every stage of the project development, guide should help towards its successful completion as per the predefined standards.

How student should carry out a project:



- 1. Define the problem
- 2. Specify the requirements
- 3. Specify the design in an understandable form (Block Diagram, Flowchart, Algorithm, etc)
- 4. Analyse the design
- 5. Select appropriate simulation tool and development board for the design.
- 6. Implement the design
- 7. Optimize the design and generate the results with optimized design.
- 8. Result representation and analysis
- 9. Prepare a document and presentation.

Report Writing

- 1. The format for report writing should be downloaded from ftp://10.3.0.3/minorprojects
- 2. The report needs to be shown to guide and committee for each review.



Program: Electronics & Commu	Semester: VI				
Course Title: Analog Integrated Circuit Design		Course Code: 23EECE301			
L-T-P: 2-0-1	Credits: 3	Contact Hours:4 hrs/week			
ISA Marks: 50	ESA Marks: 50	Total Marks: 100			
Teaching Hours: 30Hrs Examination Duration: 3 Hrs					

- 1. **Basic MOS Device Physics:** General considerations, MOS I/V characteristics, second order effects and MOS device models.
- 2. Current Mirrors: Basic current Mirror, Widlar, Cascode and Wilson Current Mirrors.
- 3. Single Stage Amplifiers: CS, CG, CD, Cascode and Folded Cascode. Frequency response curves

Unit II

- 4. **Differential Amplifiers:** Differential Amplifier, 5 pack differential Amplifier, CMRR, PSRR
- 5. **Op-Amp:** Performance parameters, Two stage (7-pack) Op-amp, Slew rate, PSRR , Noise in Op-amps
- 6. **Compensation Technique:** Nyquist stability Criterion, Gain and Phase margins, Compensation of Two stage op-amp and Dominant pole compensation technique.

Unit III

- 1. **Reference Circuits:** Current reference, startup circuits, Bandgap reference circuit, Current mode Bandgap reference.
- 2. **Comparators:** Basic Comparator architecture, non-idealities-offset error, bandwidth consideration, Dynamic comparator.

Text Books

- 1. B Razavi 'Design of Analog CMOS Integrated Circuits' First Edition McGraw Hill 2001
- 2. Phillip. E. Allen, Douglas R. Holberg, "CMOS Analog circuit Design" Oxford University Press, 2002.

Reference Books:

1. Baker, Li, Boyce, "CMOS: Circuit Design, Layout and Simulation", Prentice Hall of India, 2000



Program: Electronics & Communication Engineering		Semester: VI
Course Title: Introduction to Deep Learning		Course Code: 23EECE322
L-T-P: 2-0-1	Credits: 3	Contact Hours:4 hrs/week
ISA Marks: 80	ESA Marks: 20	Total Marks: 100
Teaching Hours: 30Hrs	Examination Duration: 3 Hrs	

Chapter No. 1.Introduction

Introduction to MP Neuron and its Geometric interpretation, Perceptron model and its Geometric interpretation. Basics of Multi-Layer Perceptron (MLP) training: Perceptron, Basic gates using MLP, Back-propagation of MLP, Activation Functions (Sigmoids, Tanh, ReLu) Handson session on Python basics, data types, vectors, matrices, matrix multiplication, plotting vectors, dot product, Implementation of MP Neuron and Perceptron Model

Chapter No. 2 Sigmoid Neuron

Challenges in MLP (vanishing and exploding gradients, slow or no convergence) Introduction to Sigmoid neuron, Mathematical interpretation, Introduction to Taylor's series, deriving the gradient descent. Handson session on Plotting sigmoid 2D, 3D, Contour plots

Unit II

Chapter No. 3. Optimization Algorithms

Optimization (Gradient Descent) Momentum, Nestrov Momentum, Advance Optimization (Adagrad, Adadelta, RMS Prop, Adam), Regularization (Dropout and its variants as a L2 regularizer) Handson session on Implementing optimization algorithms: Gradient Descent(GD), Momentum, Nesterov Accelerated GD, Mini Batch GD, Adagrad, RMS Prop, Adam, Vectorised GD algorithms

Chapter No. 4. Convolution Neural Networks and its Applications

2D Convolutions, Strides, One layer of a convolution network, ReLu and pooling, Example of a ConvNet, Training CNNs, Classic CNN Networks for classification (LeNet, AlexNet, VGG, ResNet), classic CNN networks for object detection (RCNN, fast RCNN and faster RCNN), classic CNN networks for semantic segmentation (SegNet, DeConvNet, Deep labs) Handson session on Introduction to Pytorch, Implementing CNNs using Pytorch

Unit III

Chapter No.5. Recurrent Neural Networks

Concept of word embedding, RNN model, Back propagation through time, Types of RNN, Vanishing gradients with RNN, Gated Recurrent Unit, Sequence to sequence learning, LSTM, Bidirectional RNN, Deep RNN.

Chapter No.6. Self-Supervised algorithms

Introduction to Auto encoders, Variational Auto Encoders and GANS

Text Books

- 1. Deep learning Ian Good fellow, Yoshua Bengio, Aaron Courville, MIT Press
- 2. Neural Networks and Deep Learning by Michael Nielsen



Program: Electronics & Communication Engineering		Semester: VI
Course Title: Architectural Desig	n of Integrated Circuits	Course Code: 23EECE302
L-T-P: 2-0-1	Credits: 3	Contact Hours: 4 hrs/week
ISA Marks: 100	ESA Marks:	Total Marks: 100
Teaching Hours: 30Hrs	Examination Duration: 3 Hrs	

Chapter No. 1. Digital Integrated Circuits

Challenges in digital design, Design metrics, Cost of Integrated circuits, ASIC, Evolution of SoC ASIC Flow Vs SoC Flow, SoC Design Challenges. Introduction to CMOS Technology, PMOS & NMOS Operation, CMOS Operation principles, Characteristic curves of CMOS, CMOS Inverter and characteristic curves, Delays in inverters, Buffer Design, Power dissipation in CMOS, CMOS Logic, Stick diagrams and Layout diagrams. Setup time, Hold Time, Timing Concepts.

Chapter No. 2. System Building Blocks

Modelling finite state Machines, Data Path and controller design, Synthesizable Verilog, Pipeline modelling

Chapter No. 3. Design and simulation of Micro - Architectural blocks

Efficient technique/s for Algorithm to Architecture Mapping, Recent Trends on Adder/Subtractor Design, Efficient VLSI Architectures for Various DSP blocks (FIR filter, CORDIC, FFT), Pipeline Implementation of Processor, Verilog Modeling of Processor

Chapter No. 4. Timing Analysis

Fundamentals of Efficient Design and Implementation strategies of Digital VLSI Design (Clock Tree synthesis, Timing Closure, Synthesis), Static Timing Analysis , Clock Skew

Reference Books:

- 1. Digital Design by Morris Mano M, 4th Edition.
- 2. Verilog HDL: A Guide to Digital Design and Synthesis by Samir Palnitkar, 2nd Edition.
- 3. Principles of VLSI RTL Design: A Practical Guide by Sapan Garg, 2011.

Tools: Questa Sim, NC Verilog, NC Sim, CVER + GTKWave, VCSMX, Modelsim for Verilog



Program: Electronics & Communication Engineering		Semester: VI
Course Title: Internet of Things	and its Applications	Course Code: 23EECE307
L-T-P: 2-0-1	Credits: 3	Contact Hours: 4 hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 30Hrs	Examination Duration: 3 Hrs	
Unit I		
Chapter No. 1. Introduction to I	оТ	
What is IoT, Genesis of IoT, IoT	and Digitization, IoT Impact, C	Convergence of IT and IoT, IoT
Challenges.		
Chapter No. 2. Physical and Log	ical Design of IoT	
Physical design of IoT, Logical de	sign of IoT, Functional blocks of	IoT, Communication models &
APIs.		
Chapter No. 3. Smart Objects: T	he "Things" in IoT	
Sensors, Actuators, and Smar	rt Objects, Sensor Networks,	Connecting Smart Objects,
Communications Criteria.		
Unit II		
Chapter No. 4. IoT design and N	Nethodology	
Purpose & Requirements Speci	fication, Process Specification,	Domain Model Specification,
Information Model Specification,	Service Specifications, IoT Leve	Specification, Functional View
Specification, Operational View	Specification, Device & Comp	oonent Integration, Application
Development.		
Chapter No. 5. IoT Physical serve	ers and Cloud Offerings	
Introduction to Cloud Storage Me	odels & Communication APIs, W	AMP – AutoBahn for IoT, Xively
Cloud for IoT, Python Web App	dication Framework – Django,	Designing a RESTful Web API,
Amazon Web Services for IoT, Sky	Net IoT Messaging Platform	
Chapter No. 6. Data and Analyt	ICS FOR IOI	
Data and Analytics for IoT, An Int	roduction to Data Analytics for I	ioi, Machine Learning, Big Data
Analytics loois and lechnology,		
Unit III Charter No. 7. Convincion		
Chapter No. 7. Securing IOT	n challangas in OT Sacurity davi	an loval convrity. Coftware loval
A brief history about 01, Commo	n challenges in OT Security, devi	ce level security, software level
Securities.		
Manufacturing: Introduction to	connected manufacturing and	architecture for the connected
factory connected factory securi	tonnecteu manufacturing, an a	architecture for the connected
Taxt Books	ty	
1 David Hanos Conzalo Sa	lauoiro Batrick Grossotato Bob	ort Barton, Joroma Hanny "JoT
I. David Harles, Gorizaio Sa	ng Tachnologias Protocols and	Lise Cases for the internet of
Things" 1st Edition De	arson Education (Cisco Press	Indian Reprint) (ISBN: 978-
9386873743)	Landon Laucation (CISCO FIESS	
2 Vijav Madisetti and Δrsh	deen Bahga "Internet of Thing	s (A Hands-on-Annroach)" 1 st
Edition, VPT 2014 (ISBN)	978-8173719547)	
Reference Books:		
1. Daniel Minoli, "Building t	he Internet of Things with IPv6	and MIPv6: The Evolving World

of M2M Communications", ISBN: 978-1-118- 47347-4, Willy Publications



- 2. Peter Waher, "Learning Internet of Things", PACKT publishing, BIRMINGHAM MUMBAI
- 3. Bernd Scholz-Reiter, Florian Michahelles, "Architecting the Internet of Things", ISBN
- 4. 978-3-642-19156-5 e-ISBN 978-3-642-19157-2, Springer



Program: Electronics & Communication Engineering		Semester: VI
Course Title: Information Theory and Coding		Course Code: 21EECE308
L-T-P: 3-0-0	Credits: 3	Contact Hours:3 hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 40Hrs	Examination Duration: 3 Hrs	

Chapter 01. Review of information theory

Basics of Information, Measure of information, Entropy.

Chapter 02. Discrete Channels

Discrete memory less Channels, Mutual information, Channel Capacity, Differential entropy and mutual information for continuous ensembles, Channel capacity Theorem.

Chapter 03.Source Coding

Encoding of the source output, Shannon's encoding algorithm. Source coding theorem, Binary, ternary and quaternary Huffman coding, Construction of instantaneous codes.

Unit II

Chapter 04. Introduction to Error Control Coding

Introduction, Types of errors, examples, Types of codes Linear Block Codes: Matrix description, Error detection and correction, Standard arrays and table look up for decoding, Generation of Hamming Codes.

Chapter 05. Binary Cycle Codes

Algebraic structures of cyclic codes, Encoding using an (n-k) bit shift register, Systematic codes, non-systematic codes, Error detection and error correction (Syndrome calculation) circuits.

Chapter 06. Convolutional codes

Convolution Codes, Time domain approach. Transform domain approach. Systematic Convolution codes, Maximum Likelihood Decoding of Convolutional codes.

Unit III

Chapter 07. Coding for burst error correction and other types of codes

Burst and random error correcting codes, cyclic codes and convolutional codes for bursts error correction, Reed soloman codes, Cyclic redundancy codes, Golay codes, Shortened cyclic codes, Burst error correcting codes. Burst and Random Error correcting codes.

Text Book (List of books as mentioned in the approved syllabus)

- 1. K. Sam Shanmugam, Digital and analog communication systems, John Wiley, 1996
- 2. Simon Haykin, Digital communication, John Wiley, 2003

References

- 1. Ranjan Bose, ITC and Cryptography, TMH(reprint 2007), 2002
- 2. Glover and Grant, Digital Communications, 2, Pearson, 2008
- 3. D Ganesh Rao, K N Haribhat, Digital Communications, Sanguine, 2009



Program: Electronics & Communication Engineering		
Course Title: Embedded Intelligent Systems		
Credits: 3	Contact Hours: 5 hrs/week	
ESA Marks: 20	Total Marks: 100	
Examination Duration: 3 Hrs		
	nication Engineering ent Systems Credits: 3 ESA Marks: 20 Examination Duration: 3 Hrs	

Basics of embedded systems

Linux Application Programming, System V IPC, Linux Kernel Internals and Architecture, Kernel Core, Linux Device Driver Programming, Interrupts & Timers, Sample shell script, application program, driver source build and execute.

Heterogeneous computing

Basics of heterogeneous computing with various hardware architectures designed for specific type of tasks, Advanced heterogeneous computing with a. Introduction to Parallel programming b. GPU programming (OpenCL) c. Open standards for heterogeneous computing (Openvx), Basic OpenCL examples - Coding, compilation and execution

ML Frameworks lab with the target device

Caffe, TensorFlow, TF Lite machine learning frameworks & architecture, Model parsing, feature support and flexibility, supported layers, advantages and disadvantages with each of these frameworks, Android NN architecture overview, Full stack compilation and execution on embedded device

Model Development and Optimization

Significance of on device AI, Quantization, pruning, weight sharing, Distillation, Various pretrained networks and design considerations to choose a particular pre-trained model, Federated Learning, Flexible Inferencing

Android Anatomy

Android Architecture, Linux Kernel, Binder, HAL Native Libraries, Android Runtime, Dalvik Application framework, Applications, IPC

Text Books:

1. Linux System Programming, by Robert Love, Copyright © 2007 O'Reilly Media Heterogeneous Computing with OpenCL, 2nd Edition by Dana Schaa, Perhaad Mistry, David R. Kaeli, Lee Howes, Benedict Gaster, Publisher: Morgan Kaufmann

Reference Books:

- 1. Deep Learning, MIT Press book, Goodfellow, Bengio, and Courville's
- 2. Beginning Android , by Wei-Meng Lee , Publisher: Wrox , O'Reilly Media

Experiment wise plan

Expt./Job	Experiment/job Details
No.	
1.	Practice programs on Linux Application Programming, system IPC
2.	Implement toolchain, linker, and loaders while building Hello World on the host, then execute on target.
3.	Basic OpenCL examples - Coding, compilation, and execution



4.	High-level language to assembly language translation – optimization and power management.
5.	Implementation of Caffe TensorFlow, TF Lite machine learning frameworks & architecture. Execution of sample programs with various pre-trained models
6.	Full stack compilation and execution on an embedded device. Quantization, pruning, weight sharing, Distillation execution with parameters.
7.	Implement basic programs in the Android framework and implement Android NN architecture.
8.	Push the ML/DL model on an Android device and run the application.
9.	Design an ML/DL model for a given problem targeted at Android devices with different architectures based on provided specifications.


Program: Electronics & Communication Engineering		Semester: VI	
Course Title: Multicore Architecture and Programming		Course Code: 23EECE340	
L-T-P: 2-0-1	Credits: 3	Contact Hours: 4 hrs/week	
ISA Marks: 80	ESA Marks: 20	Total Marks: 100	
Teaching Hours: 30Hrs	Examination Duration: 3 Hrs		

Chapter No. 1: Introduction to Multicore

Drivers for Multicore Architectures: Low power, Performance/Throughput and need for memory bandwidth – Limits of single core computing – Moore's law - Limits to Instruction Level Parallelism (ILP) – Power and heat dissipation issue – Increased amount of data to process – Evolution from traditional System-On-Chip (SoC) to MPSoCs (Multi processor System-On-Chips) - Need for Multicore controllers in Automotive domain

Chapter No. 2: Multicore Architecture

Dependent Multicore software and hardware architectures –Multicore hardware architecture overview: Heterogeneous and Homogenous Multicore hardware – Communication between hardware processing elements: Point-to-point connections, Shared buses, On-chip cross bar, Network-On-Chip (NoC) - Memory access in Multicore architectures: Symmetric Multi-Processing (SMP), Asymmetric Multi processing aka NUMA (Add pros and cons)– Multicore architecture specific to applications - Example Multicore hardware used in Automotive – Infineon Tricore series, ST devices

Chapter No. 3: Scheduling concepts and OS aspects

What is Scheduling? – Static and Dynamic Scheduling - Scheduling algorithms: Rate Monotonic Scheduling (RMS), Fixed priority preemptive scheduling, Round robin scheduling, Earliest deadline first, First come First serve – Process and threads - What is pre-emption? Why is it needed?- Types of Multicore Scheduling: Global, Semi-partitioned and Partitioned –OS for General purpose and Real time systems - Scheduling in Single core vs Scheduling in Multicore – Timing Jitter

Chapter No. 4:Concurrency and Parallelism

Amdahl's law – Need for Parallelism – Concurrency Fundamentals – Data parallelism, Functional Parallelism, loop Parallelism – Dependencies – Producer consumer`— Need for Synchronization, Loop dependencies–Shared resources – Caching aspects - Problems with no synchronization - Synchronization primitives – Semaphore, Mutex, spinlocks, Test and Set, Compare and swap– Synchronization related issues and how to avoid them: Data races, Livelocks, Deadlock, Non-atomic operations

Chapter 5: Advanced Multicore topics – Introduction/Overview

Multicore timing analysis - Timing simulation: Why it is needed? – WCET (Worst Case Execution Time) analysis – Schedulability analysis – Additional challenges in Multicore - Tools used in automotive: Timing architect, ChronSIM, Sym TA/S- Deterministic behaviour – Logical Execution Time (LET)

References:

- 1. Highly Recommended: Real world Multicore embedded systems Bryon Moyer
- 2. Highly Recommended for Embedded system and Real Time basics Programming *Embedded* Systems with C and GNU Development Tools Michael Barr



Program: Electronics & Communication Engineering		Semester: VI
Course Title: OOPS using C++		Course Code: 23EECE321
L-T-P: 2-0-1	Credits: 3	Contact Hours: 4 hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 50Hrs	Examination Duration: 3 Hrs	

Chapter 1: Fundamental concepts of object oriented programming

Introduction to object oriented programming, Programming Basics (keywords, identifiers, variables, operators, classes, objects), Arrays and Strings Functions/ methods (parameter passing techniques)

Chapter 2: OOPs Concepts

Overview of OOPs Principles, Introduction to classes & objects, Creation & destruction of objects, Data Members, Member Functions, Constructor & Destructor, Static class member, Friend class and functions, Namespace

Unit II

Chapter 3: Inheritance

Introduction and benefits, Abstract class, Aggregation: classes within classes Access Specifier, Base and Derived class Constructors, Types of Inheritance. Function overriding

Chapter 4: Polymorphism

Virtual functions, Friend functions, static functions, this pointer

Unit III

Chapter 5: Exception Handling

Introduction to Exception, Benefits of Exception handling, Try and catch block, Throw statement, Pre-defined exceptions in C++,Writing custom Exception class

Chapter 6: I/O Streams

C++ Class Hierarchy, File Stream, Text File Handling, Binary File Handling Error handling during file operations, Overloading << and >> operators

Text Book

1. Robert Lafore, "Object oriented programming in C++", 4th Edition, Pearson education, 2009.

References

- 1. Lippman S B, Lajorie J, Moo B E, C++ Primer, 5ed, Addison Wesley, 2013.
- 2. Herbert Schildt: The Complete Reference C++, 4th Edition, Tata McGraw Hill



Program: Electronics & Communication Engineering		Semester: VI
Course Title: Multimodal Machine Learning		Course Code: 23EECE327
L-T-P: 2-0-1	Credits: 3	Contact Hours: 4 hrs/week
ISA Marks: 100	ESA Marks:	Total Marks: 100
Teaching Hours: 30Hrs	Examination Duration: 3 Hrs	

Chapter No.1 Introduction

Multimodal AI technologies, Multimodal behaviour and signals, Dimensions of heterogeneity, Multimodal data types (text, audio and images)

Chapter No. 2 Challenges in multimodality

Representation, alignment, reasoning, generation, Transference and quantification

Chapter No. 3 Tools for multimodal learning

Introduction to deep learning techniques Convolutional Neural Networks (CNNs), Recurrent Neural Networks (RNNs), Auto Encoders and transformer- based models, and their application to multimodal data.

Unit II

Chapter No. 4 Natural Language Processing (NLP)

Techniques for processing and analyzing textual data, including tokenization, embedding, and language models including BERT and GPT

Chapter No. 5 Computer Vision

Techniques for processing and analyzing image and video data, including object detection, segmentation, and classification

Chapter No. 6 Audio processing

Techniques for processing and analyzing audio data, including speech recognition, speaker identification, and music classification

Unit III

Chapter No. 7 Knowledge distillation models

Response based, Feature based and Relation based knowledge distillation models

Chapter No. 8 Evaluation and optimization

Techniques for evaluating multimodal machine learning models and optimizing their performance, including metrics, cross-validation, and hyperparameter tuning



Program: Electronics & Communication Engineering		
Course Title: Digital Image Processing		
Credits: 3	Contact Hours: 4 hrs/week	
ESA Marks: 20	Total Marks: 100	
Teaching Hours: 30Hrs Examination Duration: 3 Hrs		
	nication Engineering essing Credits: 3 ESA Marks: 20 Examination Duration: 3 Hrs	

Chapter 1. Introduction

Introduction to Image processing and Computer Vision. Application domains of Image processing and computer vision. Image acquisition, sampling, quantization, temporal properties of vision.

Chapter 2. Image Formation

Fundamental Concepts of Image Formation: Radiometry, Geometric Transformations, Geometric Camera Models. Camera Calibration, Image Formation in a Stereo Vision Setup, Image Reconstruction from a Series of Projections

Unit II

Chapter 3. Image Transforms

2D orthogonal and unitary transforms, DFT, DCT, DST, KLT transforms

Chapter 4. Image Enhancement

Histograms modelling, spatial operations, transform operations, multispectral image enhancement

Chapter 5. Image Descriptors and Features

Texture Descriptors, Colour Features, Edges/Boundaries. Interest or Corner Point Detectors, Histogram of Oriented Gradients, Scale Invariant Feature Transform, Speeded up Robust Features, Saliency

Unit III

Chapter 6. Filtering and Restoration

Colour Image Processing, Image Segmentation, Image observation models, Inverse and wiener filtering

Text Books (List of books as mentioned in the approved syllabus)

Rafael C. Gonzalez & Richard E. Woods, "Digital Image Processing", Third Edition, Pearson.
 NOC | Computer Vision and Image Processing - Fundamentals and Applications (nptel.ac.in)

References:

1. A.K. Jain, "Fundamentals of Digital Image Processing", Pearson Education (Asia) Pvt. Ltd.



Program: Electronics & Communication Engineering		Semester: VII
Course Title: Wireless and Mobile Networks		Course Code: 24EECC403
L-T-P: 2-0-1	Credits: 3	Contact Hours: 4 hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 30Hrs	Examination Duration: 3 Hrs	

Chapter No. 1. Local Area Networks

Error-detection and correction techniques, multiple access links and protocols, Link-Layer Addressing and ARP, Ethernet 802.3, Token ring 802.5, FDDI and LAN standards, Link-Layer Switches, Virtual Local Area Networks (VLANS).

Chapter No. 2. Wireless Networks

Introduction, Wireless Links and Network Characteristics, CDMA, WiFi: 802.11 Wireless LANs, The 802.11 Architecture, The 802.11 MAC Protocol, The IEEE 802.11 Frame, Mobility in the Same IP Subnet, Advanced Features in 802.11, Personal Area Networks: Bluetooth and Zigbee.

Unit II

Chapter No. 3 Cellular Networks

An Overview of Cellular Network Architecture, 3G Cellular Data Networks: Extending the Internet to Cellular Subscribers, 4G LTE Cellular Networks: Architecture and Elements, LTE Protocols Stacks, LTE Radio Access Network, Additional LTE Functions: Network Attachment and Power Management, The Global Cellular Network: A Network of Networks

Chapter No. 5: 5G Cellular Networks-1

Basics of 5G Technology: Overview of 5G architecture, Layered Architecture, Key features and requirements, Spectrum considerations for 5G

Unit III

Chapter No. 6: 5G Cellular Networks-2

Mobility Management: Principles, Device Mobility: a Network-layer Perspective, Home Networks and Roaming on Visited Network, Direct and Indirect Routing to/from a Mobile Device, Mobility Management in Practice, Mobility Management in 5G Networks Mobile IP, Wireless and Mobility: Impact on Higher-Layer Protocols

Text Book (List of books as mentioned in the approved syllabus)

- 1. Kurose & Ross, Computer Networking A Top-Down Approach, 6th edition, PEARSON, 2013.
- 2. 5G NR: The Next Generation Wireless Access Technology & quot;, Erik Dahlman, Stefan Parkvall, Johan Sköld , Academic Press

References

- 1. Behrouz A. Forouzan, Data Communications and Networking , 4th Edition, Tata McGra, 2006
- 2. Larry L. Peterson and Bruce S. Davie, Computer Networks A Systems Approach, : 4th Edition, Elsevier, 2007

Back to Semester VII



Program: Electronics & Communication Engineering		Semester: VII
Course Title: Senior Design Project		Course Code: 20EECW401
L-T-P: 0-0-6	Credits: 6	Contact Hours: 12 hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours:	Examination Duration: 3 Hrs	

- Smart City
- Connected Cars
- Home Automation
- Health care
- Smart energy
- Automation of Agriculture

Guide lines for selection of a project:

- The project needs to encompass the concepts learnt in the previous semesters, so that the student will learn to integrate, the knowledge base acquired to provide a solution to the defined problem statement of the project work.
- Student can select a project which leads to a product or model or prototype.
- Time plan: Effort to do the project should be between 60-70 Hrs per team, which includes self-study of an individual member (80-100 Hrs) and team work (40-50 hrs).

Learning overhead should be 20-25% of total project development time.

Criteria for group formation:

- 3-4 students in a team.
- Role of teammates: Team lead and members.

Allocation of Guides and Mentors for the projects: Every Project batch will be allocated with one faculty.

Details of the project batches:

- Number of faculty members: 50
- Number of students:3-4 students in a team.

Role of a Guide

The primary responsibility of the guide is to help students to understand the meaning and need of various stages in the implementation of the project. At every stage of the project development, guide should help towards its successful completion as per the predefined standards.

How student should carry out a project:

- Define the problem.
- Specify the requirements.
- Specify the design in the understandable form (Block Diagram, Flowchart, Algorithm, etc).

KLE Technological University Creating Value, Leveraging Knowledge

- Analyze the design and identify hardware and software components separately.
- Select appropriate simulation tool and development board for the design.
- Implement the design.
- Optimize the design and generate the results.
- Result representation and analysis.
- Prepare a document and presentation.

Report Writing

• The format for report writing should be downloaded from ftp://10.3.0.3/projects

• The report needs to show to the respective guide and committee for each review. Evaluation Scheme

- - Internal semester assessment (ISA)
 Evaluation is done based on the evaluation rubrics
 - Evaluation is done based on the evaluation rubrics given in Table 1
 Broject shall be reviewed and evaluated by the concerned Guide for EG
 - Project shall be reviewed and evaluated by the concerned Guide for 50% of the marks.
 - The review committee for 50% of the marks shall evaluate project.

Back to Semester VII



Program: Electronics & Communication Engineering		Semester: VII
Course Title: CIPE & EVS		Course Code: 15EHSA401
L-T-P: 2-0-0	Credits: Audit	Contact Hours: 2 hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 30Hrs	Examination Duration: 3 Hrs	

Chapter No. 1 Features of Indian Constitution

Features of Indian Constitution, Preamble to the constitution of India, Fundamental rights under Part III – details of Exercise of rights, Limitations & Important cases. Berubari Union and Exchange of Enclaves, Kesavan and Bharati vs. UOI, Maneka Gandhi vs. UOI, Air India Ltd. vs. Nargees Meerza, T.M.A. Pai Foundation v. St. of Karnataka, M.C. Mehta vs. UOI etc.,

Chapter No. 2 Relevance of Directive principles of State Policy

Relevance of Directive principles of State Policy under Part IV, Fundamental duties & their significance. Sarla Mudgal v. UOI

Chapter No. 3 Union

Union – President, Vice President, Union Council of Ministers, Prime Minister, Parliament & the Supreme Court of India.

Chapter No.4 State

State – Governors, State Council of Ministers, Chief Minister, State Legislature and Judiciary.

Chapter No. 5 Constitutional Provisions for Scheduled Castes & Tribes

Constitutional Provisions for Scheduled Castes & Tribes, Women & Children & Backward classes, Emergency Provisions.

Chapter No. 6 Electoral process

Electoral process, Amendment procedure, 42nd, 44th and 86th Constitutional amendments.

Unit II

Chapter No. 7 Scope & Aims of Engineering Ethics

Scope & Aims of Engineering Ethics: Meaning and purpose of Engineering Ethics, Responsibility of Engineers, Impediments to responsibility, Honesty, Integrity and reliability, risks, safety & liability in engineering. Bhopal Gas Tragedy, Titanic case.

Chapter No. 8 Intellectual Property Rights

Intellectual Property Rights (IPRs)- Patents, Copyright and Designs

Chapter No. 9 Ethical perspectives of professional bodies

Ethical perspectives of professional bodies- IEEE, ASME, NSPE and ABET, ASCE etc. **Unit III**

Chapter No. 10 Effects of human activities on environment

Effects of human activities on environment - Agriculture, Housing, Industry, Mining, and Transportation activities, Environmental Impact Assessment, Sustainability and Sustainable Development.

Chapter No. 11 Environmental Protection

Environmental Protection – Constitutional Provisions and Environmental Laws in India.

Text Book (List of books as mentioned in the approved syllabus)

- 1. Dr. J. N. Pandey, "Constitutional Law of India", Central Law Agency, 2005
- 2. Dr. M.K. Bhandari, "Law relating to Intellectual Property Rights", Central Law Publications, Allahabad, 2010.



3. Charles E. Harris and others, "Engineering Ethics: Concepts and Cases", Thomson Wadsworth, 2003

References

- 1. Durga Das Basu, "Introduction to the Constitution of India", Prentice-hall EEE, 2001
- 2. Mike Martin and Ronald Schinzinger, "Ethics in Engineering", Tata McGraw-Hill Publications.

Back to Semester VII



Program: Electronics & Communication Engineering		
Course Title: System Verilog for Verification		
Credits: 3	Contact Hours:4 hrs/week	
ESA Marks:	Total Marks: 100	
Examination Duration: 3 Hrs		
	nication Engineering Verification Credits: 3 ESA Marks: Examination Duration: 3 Hrs	

Chapter No. 1. Verification Concepts

Concepts of verification, importance of verification, Stimulus vs Verification, functional verification, test bench generation, functional verification approaches, typical verification flow, stimulus generation, direct testing, Coverage: Code and Functional coverage, coverage plan.

Chapter No. 2. System Verilog – Language Constructs

System Verilog constructs - Data types: two-state data, strings, arrays: queues, dynamic and associative arrays, Structs, enumerated types. Program blocks, module, interfaces, clocking blocks, mod-ports.

Chapter No. 3. System Verilog – Classes & Randomization

SV Classes: Language evolution, Classes and objects, Class Variables and Methods, Class instantiation, Inheritance, and encapsulation, Polymorphism. Randomization: Directed Vs Random Testing. Randomization: Constraint Driven Randomization.

Chapter No. 4. System Verilog – Assertions & Coverage

Assertions: Introduction to Assertion based verification, Immediate and concurrent assertions. Coverage driven verification: Motivation, Types of coverage, Cover Group, Cover Point, Cross Coverage, Concepts of Binning and event sampling.

Chapter No. 5. Building Testbench

Layered testbench architecture. Introduction to Universal Verification Methodology, Overview of UVM Base Classes and simulation phases in UVM and UVM macros. Unified messaging in UVM, UVM environment structure, Connecting DUT- Virtual Interface

Reference Books

- 1. System Verilog LRM
- 2. Chris Spear, Gregory J Tum bush System Verilog for verification a guide to learning the testbench language features Springer, 2012

Tools: Questa Sim, NC Verilog, NC Sim, CVER + GTK Wave, VCSMX, Mode Isim for Verilog



Program: Electronics & Commu	nication Engineering	Semester: VII
Course Title: Speech Processing		Course Code: 24EECE422
L-T-P: 2-0-1	Credits: 3	Contact Hours: 4 hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 30Hrs	Examination Duration: 3 Hrs	

Chapter 1: Introduction

Speech production and perception, nature of speech; short-term processing: need, approach, time, frequency and time-frequency analysis.

Chapter 2: Short-term Fourier transform (STFT)

Overview of Fourier representation, non-stationary signals, development of STFT, transform and filter-bank views of STFT.

Chapter 3: Cepstrum analysis

Basis and development, delta, delta-delta and mel-cepstrum, homomorphic signal processing, real and complex cepstrum.

Unit II

Chapter No 4: Linear Prediction (LP) analysis

Basis and development, Levinson-Durbin's method, normalized error, LP spectrum, LP cepstrum, LP residual.

Chapter 5: Sinusoidal analysis

Basis and development, phase unwrapping, sinusoidal analysis and synthesis of speech.

Chapter 6: Mathematical models and Applications

Gaussian mixture models and hidden Markov models

Unit III

Chapter No 7: Introduction to Bayesian Approach

Bayesian classification, Bayesian Learning, Bayes Optimal Classifier, Naive Bayes Classifier and Bayesian Network.

Chapter 8: Introduction to Speech Technologies

Automatic Speech recognition, speaker recognition, speaker diarization, speech synthesis, language and dialect identification and speech coding

Text Books:

- 1. L.R. Rabiner and R.W. Schafer, Digital Processing of Speech Signals Pearson Education, Delhi, India, 2004
- 2. J. R. Deller, Jr., J. H. L. Hansen and J. G. Proakis Discrete-Time Processing of Speech Signals, Wiley-IEEE Press, NY, USA, 1999.

Reference Books:

- 1. D. O'Shaughnessy, Speech Communications: Human and Machine, Second Edition, University Press, 2005.
- 2. T. F. Quatieri, "Discrete time processing of speech signals", Pearson Education, 2005.



3. L. R. Rabiner, B. H. Jhuang and B. Yegnanarayana, "Fundamentals of speech recognition", Pearson Education, 2009.



Program: Electronics & Communication Engineering		Semester: VII
Course Title: Multimedia Communication		Course Code: 18EECE410
L-T-P: 3-0-0	Credits: 3	Contact Hours:3 hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 40Hrs	Examination Duration: 3 Hrs	

Chapter 1: Introduction to Multimedia: Multimedia and Hyper media, WWW, overview of multimedia software tools.

Chapter 2: Graphics and Image representation: Graphics / Image data types, Popular file formats.

Chapter 3: Fundamental concepts in video: Types of video signals, analog video, digital video.

Chapter 4: Basics of digital audio: Digitization of sound, MIDI, Quantization and transmission of audio.

Unit II

Chapter 4: Lossless compression algorithms: Introduction, run-length coding, variable length coding, dictionary based coding, arithmetic coding, lossless image compression.

Chapter 5: Lossy compression algorithms: Introduction, distortion measures, quantization, transform coding, wavelet based coding, wavelet packets, embedded zero tree of wavelet coefficients.

Chapter 6: Image compression standards: The JPEG standard, The JPEG2000 standard, The JPEG-LS standard, Bi level image compression standard.

Unit III

Chapter 7: Basics video compression techniques: Overview, video compression based on motion compensation, H.261

Chapter 8: Overview of MPEG-1, 2 4 and 7.

Text Books

1. Ze-Nian Li & Mark S Drew, "Fundamentals of multimedia", Pearson Education, 2004.

References

- 1. Ralf Steinmetz & Kalra Nahrstedt , "Multimedia: Computing, Communication & Applications", Pearson Education, 2004
- 2. K R Rao, Zoran S Bojkovic, Dragord A Milovanvic, Pearson education, "Multimedia communication systems: Techniques, Standards, & Networks", Second Indian reprint, 2004.



Program: Electronics & Communication Engineering		Semester: VII
Course Title: Physical Design - Analog		Course Code: 18EECE419
L-T-P: 0-0-3	Credits: 3	Contact Hours:6 hrs/week
ISA Marks: 100	ESA Marks:	Total Marks: 100
Teaching Hours: 40Hrs	Examination Duration: 3 Hrs	

Chapter No 1. Standard cell Layout creation

Layout Practice Sessions (DRC/LVS Dirty layout), Understanding verification errors, Error debugging skills, Hands on experience of using layout editor, Quality of the layout, Half DRC rules, Mega module creation.

Chapter No 2. Analog layout

Importance of performance in Analog layout, Importance of floor planning and placement, Attributes need to be taken care during routing stage, Introduction to DRC, LVS, Density and RCX.

Chapter No 3. Matching

Introduction to mismatch concepts, Causes for mismatch, Types of mismatch, Rules for matching, Activities.

Chapter No 4. Guard ring and shielding

Guard ring- need of guard ring, What is guard ring, Usage of guard ring shielding- What is shielding, Types of shielding, importance of shielding.

Chapter No 5. Physical design of amplifier and buffer

Applying the studied concepts and doing layout, Prioritising the constraints given, Quality checks, Buddy reviews and implementations, Documentation

References

- 1. The Art of Analog Layout Alan Hastings
- 2. CMOS IC layout Dan Clien
- 3. IC Layout Basics Chris saint and Judy saint



Course Title: CMOS ASIC DesignCourse Code: 24EECE420L-T-P: 2-0-1Credits: 3Contact Hours: 4 hrs/weekISA Marks: 100ESA Marks:Total Marks: 100Teaching Hours: 30HrsExamination Duration: 3 HrsChapter No. 1. Introduction: Design of combinational and sequential logic gates in CMOS. Layout and characterization of standard cells. Verilog for representing are level netlists.Chapter No. 2. Timing AnalysisSequential circuit timing and static timing analysis. Cell and net delays and cross-talk. Rationale and implementation of scan chains for testing standard-cell based logic circuits. Timing Verification: Setup Timing Check, Hold Timing Check, Timing across Clock DomainsChapter No. 3: Physical design Verification: Setup Timing Check, Hold SAISC: scan insertion, placement, and clock tree synthesis and routing. Netlist transformations at each step of the physical design process. Net parasitic and parasitic extraction. Use of PLLs for clock generation and de-skew.Chapter No. 4. Standard Data formatsStandard data formats for representing technology and design: LEF, Liberty, SDC, DEF and SPEF. Clock gating and power gating for reduction of device power consumption. Design for reliability: electro- migration, wire self heat and ESD checks and fixes.Reference Books: 1. The Design & Analysis of VLSI Circuits, L. A. Glassey & D. W. Dobbepahl, Addison Wesley Pub Co. 1985.2. H. Bhatnagar, Advanced ASIC Chip Synthesis Using Synosys Design Compiler Physical Compiler and Prime Time, 2nd edition, 2001.3. Static Timing Analysis for Nano meter Designs A Practical Approach, J. Bhasker • Rakesh Chadha, SpringerScience+Business Media, LLC 2009Tools: Cadence Innovous, Encounter <th colspan="2">Program: Electronics & Communication Engineering</th> <th>Semester: VII</th>	Program: Electronics & Communication Engineering		Semester: VII
L-T-P: 2-0-1Credits: 3Contact Hours: 4 hrs/weekISA Marks: 100ESA Marks:Total Marks: 100Teaching Hours: 30HrsExamination Duration: 3 HrsChapter No. 1. Introduction: Design of combinational and seque-tial logic gates in CMOS. Layout and characterization of standard cells. Verilog for representing gate level netlists.Chapter No. 2. Timing Analysis Sequential circuit timing and static timing analysis. Cell and net elays and cross-talk. Rationale and implementation of scan chains for testing standard-cell based logic circuits. Timing Verification: Setup Timing Check, Hold Timing Check, Timing across Clock DomainsChapter No. 3: Physical design Verification: Setup Timing Check, Hold Timing Check, Timing across Clock DomainsChapter No. 4. Standard-cell based CMOS ASICs: scan insertion, placement, and clock tree synthesis and routing. Netlist tra-sformations at each step of the physical design process. Net parasitic and parasitic extraction. Use of PLLs for clock generation. Design for reliability: electro- migration, wire self heat and ESD checks and fixes.Chapter No. 5. Packaging A noverview of package design - reduction of device power consumption. Design for reliability: electro- migration, wire self heat and ESD checks and fixes.Reference Books: 1. The Design & Analysis of LSI Circuits, L. A. Glassey & D. W. Dobbepahl, Addison Wesley Pub Co. 1985.2. H. Bhatnagar, Advanced ASIC Chip Synthesis Using SAProach, J. Bhasker • Rakesh Chadha, SpringerScience+Business Media, LLC 2009Tools: Cadence Innovous, Encourt	Course Title: CMOS ASIC Design		Course Code: 24EECE420
ISA Marks: 100ESA Marks:Total Marks: 100Teaching Hours: 30HrsExamination Duration: 3 HrsChapter No. 1. Introduction: Design of combinational and sequential logic gates in CMOS. Layout and characterization of standard ⊂ells. Verilog for representing gatevel netlists.Chapter No. 2. Timing AnalysisSequential circuit timing and statisming analysis. Cell and negres and cross-talk. Rationale and implementation of scan chains for testing standard-cell based logic circuits. Timing Verification: Setup Timing Check, Hold Timing Check, Timing arorss Clock DomainsChapter No. 3: Physical design Verification: Setup Timing Check, Hold Timing Check, Timing arorss Clock DomainsChapter No. 3: Physical design of standard-cell based CMOS ASICs: scan insertion, placement, and clock tree synthesis and routing. Netlist transformations at each step of the physical design process. Net parasitic and parasitic extraction. Use of PLLs for clock generation and de-skew.Chapter No. 4. Standard Data TorretsStandard data formats for represuring technology and design: LEF, Liberty, SDC, DEF and SPEF. Clock gating and power gating for reduction of device power consumption. Design for reliability: electro- migration, wire self heat and ESD checks and fixes.An overview of package design and implementation and system kerter timing.Reference Books: 1. The Design & Analysis of VLSI Circuits, L. A. Glassey & D. W. Dobbepahl, Addison Wesley Pub Co. 1985.2. H. Bhatnagar, Advanced ASIC Chip Synthesis Using Synopsys Design Compiler Physical Compiler and Prime Time, 2nd edition, 2001.3. Static Timing Analysis for Nano meter Designs A Practical Approach, J. Bhasker • Rakesh Chadha, SpringerScience+business Media, LLC 2009Tools: Cadence Innovous, Encour	L-T-P: 2-0-1	Credits: 3	Contact Hours: 4 hrs/week
Teaching Hours: 30HrsExamination Duration: 3 HrsChapter No. 1. Introduction: Design of combinational and sequential logic gates in CMOS. Layout and characterization of standard cells. Verilog for representing gate level netlists.Chapter No. 2. Timing AnalysisSequential circuit timing and static timing analysis. Cell and net delays and cross-talk. Rationale and implementation of scan chains for testing standard-cell based logic circuits. Timing Verification: Setup Timing Check, Hold Timing Check, Timing across Clock DomainsChapter No. 3: Physical designPhysical design of standard-cell based CMOS ASICs: scan insertion, placement, and clock tree synthesis and routing. Netlist transformations at each step of the physical design process. Net parasitic and parasitic extraction. Use of PLLs for clock generation and de-skew.Chapter No. 4. Standard Data formatsStandard data formats for representing technology and design: LEF, Liberty, SDC, DEF and SPEF. Clock gating and power gating for reduction of device power consumption. Design for reliability: electro- migration, wire self heat and ESD checks and fixes.Chapter No. 5. Packaging An overview of package design and implementation and system level timing.Reference Books: 1. The Design & Analysis of VLSI Circuits, L. A. Glassey & D. W. Dobbepahl, Addison Wesley Pub Co. 1985.2. H. Bhatnagar, Advanced ASIC Chip Synthesis Using Synopsys Design Compiler Physical Compiler and Prime Time, 2nd edition, 2001.3. Static Timing Analysis for Nano meter Designs A Practical Approach, J. Bhasker • Rakesh Chadha, SpringerScience+Business Media, LLC 2009Tools: Cadence Innovous, Encourter	ISA Marks: 100	ESA Marks:	Total Marks: 100
 Chapter No. 1. Introduction: Design of combinational and sequential logic gates in CMOS. Layout and characterization of standard cells. Verilog for representing gate level netlists. Chapter No. 2. Timing Analysis Sequential circuit timing and static timing analysis. Cell and net delays and cross-talk. Rationale and implementation of scan chains for testing standard-cell based logic circuits. Timing Verification: Setup Timing Check, Hold Timing Check, Timing across Clock Domains Chapter No. 3: Physical design Physical design of standard-cell based CMOS ASICs: scan insertion, placement, and clock tree synthesis and routing. Netlist transformations at each step of the physical design process. Net parasitic and parasitic extraction. Use of PLLs for clock generation and de-skew. Chapter No. 4. Standard Data formats Standard data formats for representing technology and design: LEF, Liberty, SDC, DEF and SPEF. Clock gating and power gating for reduction of device power consumption. Design for reliability: electro- migration, wire self heat and ESD checks and fixes. Chapter No. 5. Packaging An overview of package design and implementation and system level timing. Reference Books: The Design & Analysis of VLSI Circuits, L. A. Glassey & D. W. Dobbepahl, Addison Wesley Pub Co. 1985. H. Bhatnagar, Advanced ASIC Chip Synthesis Using Synopsys Design Compiler Physical Compiler and Prime Time, 2nd edition, 2001. Static Timing Analysis for Nano meter Designs A Practical Approach, J. Bhasker • Rakesh Chadha, SpringerScience+Business Media, LLC 2009 	Teaching Hours: 30Hrs	Examination Duration: 3 Hrs	
 and characterization of standard cells. Verilog for representing gate level netlists. Chapter No. 2. Timing Analysis Sequential circuit timing and static timing analysis. Cell and net delays and cross-talk. Rationale and implementation of scan chains for testing standard-cell based logic circuits. Timing Verification: Setup Timing Check, Hold Timing Check, Timing across Clock Domains Chapter No. 3: Physical design Physical design of standard-cell based CMOS ASICs: scan insertion, placement, and clock tree synthesis and routing. Netlist transformations at each step of the physical design process. Net parasitic and parasitic extraction. Use of PLLs for clock generation and de-skew. Chapter No. 4. Standard Data formats Standard data formats for representing technology and design: LEF, Liberty, SDC, DEF and SPEF. Clock gating and power gating for reduction of device power consumption. Design for reliability: electro- migration, wire self heat and ESD checks and fixes. Chapter No. 5. Packaging An overview of package design and implementation and system level timing. Reference Books: The Design & Analysis of VLSI Circuits, L. A. Glassey & D. W. Dobbepahl, Addison Wesley Pub Co. 1985. H. Bhatnagar, Advanced ASIC Chip Synthesis Using Synopsys Design Compiler Physical Compiler and Prime Time, 2nd edition, 2001. Static Timing Analysis for Nano meter Designs A Practical Approach, J. Bhasker • Rakesh Chadha, SpringerScience+Business Media, LLC 2009 	Chapter No. 1. Introduction: Des	ign of combinational and sequer	ntial logic gates in CMOS. Layout
 Chapter No. 2. Timing Analysis Sequential circuit timing and static timing analysis. Cell and net delays and cross-talk. Rationale and implementation of scan chains for testing standard-cell based logic circuits. Timing Verification: Setup Timing Check, Hold Timing Check, Timing across Clock Domains Chapter No. 3: Physical design Physical design of standard-cell based CMOS ASICs: scan insertion, placement, and clock tree synthesis and routing. Netlist transformations at each step of the physical design process. Net parasitic and parasitic extraction. Use of PLLs for clock generation and de-skew. Chapter No. 4. Standard Data formats Standard data formats for representing technology and design: LEF, Liberty, SDC, DEF and SPEF. Clock gating and power gating for reduction of device power consumption. Design for reliability: electro- migration, wire self heat and ESD checks and fixes. Chapter No. 5. Packaging An overview of package design and implementation and system level timing. Reference Books: The Design & Analysis of VLSI Circuits, L. A. Glassey & D. W. Dobbepahl, Addison Wesley Pub Co. 1985. H. Bhatnagar, Advanced ASIC Chip Synthesis Using Synopsys Design Compiler Physical Compiler and Prime Time, 2nd edition, 2001. Static Timing Analysis for Nano meter Designs A Practical Approach, J. Bhasker • Rakesh Chadha, SpringerScience+Business Media, LLC 2009 	and characterization of standard	cells. Verilog for representing ga	ate level netlists.
 Sequential circuit timing and static timing analysis. Cell and net delays and cross-talk. Rationale and implementation of scan chains for testing standard-cell based logic circuits. Timing Verification: Setup Timing Check, Hold Timing Check, Timing across Clock Domains Chapter No. 3: Physical design Physical design of standard-cell based CMOS ASICs: scan insertion, placement, and clock tree synthesis and routing. Netlist transformations at each step of the physical design process. Net parasitic and parasitic extraction. Use of PLLs for clock generation and de-skew. Chapter No. 4. Standard Data formats Standard data formats for representing technology and design: LEF, Liberty, SDC, DEF and SPEF. Clock gating and power gating for reduction of device power consumption. Design for reliability: electro- migration, wire self heat and ESD checks and fixes. Chapter No. 5. Packaging An overview of package design and implementation and system level timing. Reference Books: The Design & Analysis of VLSI Circuits, L. A. Glassey & D. W. Dobbepahl, Addison Wesley Pub Co. 1985. H. Bhatnagar, Advanced ASIC Chip Synthesis Using Synopsys Design Compiler Physical Compiler and Prime Time, 2nd edition, 2001. Static Timing Analysis for Nano meter Designs A Practical Approach, J. Bhasker • Rakesh Chadha, SpringerScience+Business Media, LLC 2009 	Chapter No. 2. Timing Analysis		
 and implementation of scan chains for testing standard-cell based logic circuits. Timing Verification: Setup Timing Check, Hold Timing Check, Timing across Clock Domains Chapter No. 3: Physical design Physical design of standard-cell based CMOS ASICs: scan insertion, placement, and clock tree synthesis and routing. Netlist transformations at each step of the physical design process. Net parasitic and parasitic extraction. Use of PLLs for clock generation and de-skew. Chapter No. 4. Standard Data formats Standard data formats for representing technology and design: LEF, Liberty, SDC, DEF and SPEF. Clock gating and power gating for reduction of device power consumption. Design for reliability: electro- migration, wire self heat and ESD checks and fixes. Chapter No. 5. Packaging An overview of package design and implementation and system level timing. Reference Books: The Design & Analysis of VLSI Circuits, L. A. Glassey & D. W. Dobbepahl, Addison Wesley Pub Co. 1985. H. Bhatnagar, Advanced ASIC Chip Synthesis Using Synopsys Design Compiler Physical Compiler and Prime Time, 2nd edition, 2001. Static Timing Analysis for Nano meter Designs A Practical Approach, J. Bhasker • Rakesh Chadha, SpringerScience+Business Media, LLC 2009 Tools: Cadence Innovous, Encounter 	Sequential circuit timing and sta	tic timing analysis. Cell and net	delays and cross-talk. Rationale
 Verification: Setup Timing Check, Hold Timing Check, Timing across Clock Domains Chapter No. 3: Physical design Physical design of standard-cell based CMOS ASICs: scan insertion, placement, and clock tree synthesis and routing. Netlist transformations at each step of the physical design process. Net parasitic and parasitic extraction. Use of PLLs for clock generation and de-skew. Chapter No. 4. Standard Data formats Standard data formats for representing technology and design: LEF, Liberty, SDC, DEF and SPEF. Clock gating and power gating for reduction of device power consumption. Design for reliability: electro- migration, wire self heat and ESD checks and fixes. Chapter No. 5. Packaging An overview of package design and implementation and system level timing. Reference Books: The Design & Analysis of VLSI Circuits, L. A. Glassey & D. W. Dobbepahl, Addison Wesley Pub Co. 1985. H. Bhatnagar, Advanced ASIC Chip Synthesis Using Synopsys Design Compiler Physical Compiler and Prime Time, 2nd edition, 2001. Static Timing Analysis for Nano meter Designs A Practical Approach, J. Bhasker • Rakesh Chadha, SpringerScience+Business Media, LLC 2009 Tools: Cadence Innovous, Encounter 	and implementation of scan of	chains for testing standard-cel	ll based logic circuits. Timing
 Chapter No. 3: Physical design Physical design of standard-cell based CMOS ASICs: scan insertion, placement, and clock tree synthesis and routing. Netlist transformations at each step of the physical design process. Net parasitic and parasitic extraction. Use of PLLs for clock generation and de-skew. Chapter No. 4. Standard Data formats Standard data formats for representing technology and design: LEF, Liberty, SDC, DEF and SPEF. Clock gating and power gating for reduction of device power consumption. Design for reliability: electro- migration, wire self heat and ESD checks and fixes. Chapter No. 5. Packaging An overview of package design and implementation and system level timing. Reference Books: The Design & Analysis of VLSI Circuits, L. A. Glassey & D. W. Dobbepahl, Addison Wesley Pub Co. 1985. H. Bhatnagar, Advanced ASIC Chip Synthesis Using Synopsys Design Compiler Physical Compiler and Prime Time, 2nd edition, 2001. Static Timing Analysis for Nano meter Designs A Practical Approach, J. Bhasker • Rakesh Chadha, SpringerScience+Business Media, LLC 2009 	Verification: Setup Timing Check	k, Hold Timing Check, Timing ac	cross Clock Domains
 Physical design of standard-cell based CMOS ASICs: scan insertion, placement, and clock tree synthesis and routing. Netlist transformations at each step of the physical design process. Net parasitic and parasitic extraction. Use of PLLs for clock generation and de-skew. Chapter No. 4. Standard Data formats Standard data formats for representing technology and design: LEF, Liberty, SDC, DEF and SPEF. Clock gating and power gating for reduction of device power consumption. Design for reliability: electro- migration, wire self heat and ESD checks and fixes. Chapter No. 5. Packaging An overview of package design and implementation and system level timing. Reference Books: The Design & Analysis of VLSI Circuits, L. A. Glassey & D. W. Dobbepahl, Addison Wesley Pub Co. 1985. H. Bhatnagar, Advanced ASIC Chip Synthesis Using Synopsys Design Compiler Physical Compiler and Prime Time, 2nd edition, 2001. Static Timing Analysis for Nano meter Designs A Practical Approach, J. Bhasker • Rakesh Chadha, SpringerScience+Business Media, LLC 2009 	Chapter No. 3: Physical design		
 synthesis and routing. Netlist transformations at each step of the physical design process. Net parasitic and parasitic extraction. Use of PLLs for clock generation and de-skew. Chapter No. 4. Standard Data formats Standard data formats for representing technology and design: LEF, Liberty, SDC, DEF and SPEF. Clock gating and power gating for reduction of device power consumption. Design for reliability: electro- migration, wire self heat and ESD checks and fixes. Chapter No. 5. Packaging An overview of package design and implementation and system level timing. Reference Books: The Design & Analysis of VLSI Circuits, L. A. Glassey & D. W. Dobbepahl, Addison Wesley Pub Co. 1985. H. Bhatnagar, Advanced ASIC Chip Synthesis Using Synopsys Design Compiler Physical Compiler and Prime Time, 2nd edition, 2001. Static Timing Analysis for Nano meter Designs A Practical Approach, J. Bhasker • Rakesh Chadha, SpringerScience+Business Media, LLC 2009 Tools: Cadence Innovous, Encounter 	Physical design of standard-cell	based CMOS ASICs: scan insert	ion, placement, and clock tree
 Chapter No. 4. Standard Data formats Standard data formats for representing technology and design: LEF, Liberty, SDC, DEF and SPEF. Clock gating and power gating for reduction of device power consumption. Design for reliability: electro- migration, wire self heat and ESD checks and fixes. Chapter No. 5. Packaging An overview of package design and implementation and system level timing. Reference Books: The Design & Analysis of VLSI Circuits, L. A. Glassey & D. W. Dobbepahl, Addison Wesley Pub Co. 1985. H. Bhatnagar, Advanced ASIC Chip Synthesis Using Synopsys Design Compiler Physical Compiler and Prime Time, 2nd edition, 2001. Static Timing Analysis for Nano meter Designs A Practical Approach, J. Bhasker • Rakesh Chadha, SpringerScience+Business Media, LLC 2009 Tools: Cadence Innovous, Encounter 	synthesis and routing. Netlist tra	ansformations at each step of the	ne physical design process. Net
 Chapter No. 4. Standard Data formats Standard data formats for representing technology and design: LEF, Liberty, SDC, DEF and SPEF. Clock gating and power gating for reduction of device power consumption. Design for reliability: electro- migration, wire self heat and ESD checks and fixes. Chapter No. 5. Packaging An overview of package design and implementation and system level timing. Reference Books: The Design & Analysis of VLSI Circuits, L. A. Glassey & D. W. Dobbepahl, Addison Wesley Pub Co. 1985. H. Bhatnagar, Advanced ASIC Chip Synthesis Using Synopsys Design Compiler Physical Compiler and Prime Time, 2nd edition, 2001. Static Timing Analysis for Nano meter Designs A Practical Approach, J. Bhasker • Rakesh Chadha, SpringerScience+Business Media, LLC 2009 Tools: Cadence Innovous, Encounter 	parasitic and parasitic extraction	. Use of PLLs for clock generatio	n and de-skew.
 Standard data formats for representing technology and design: LEF, Liberty, SDC, DEF and SPEF. Clock gating and power gating for reduction of device power consumption. Design for reliability: electro- migration, wire self heat and ESD checks and fixes. Chapter No. 5. Packaging An overview of package design and implementation and system level timing. Reference Books: The Design & Analysis of VLSI Circuits, L. A. Glassey & D. W. Dobbepahl, Addison Wesley Pub Co. 1985. H. Bhatnagar, Advanced ASIC Chip Synthesis Using Synopsys Design Compiler Physical Compiler and Prime Time, 2nd edition, 2001. Static Timing Analysis for Nano meter Designs A Practical Approach, J. Bhasker • Rakesh Chadha, SpringerScience+Business Media, LLC 2009 Tools: Cadence Innovous, Encounter 	Chapter No. 4. Standard Data fo	rmats	
 Clock gating and power gating for reduction of device power consumption. Design for rehability: electro- migration, wire self heat and ESD checks and fixes. Chapter No. 5. Packaging An overview of package design and implementation and system level timing. Reference Books: The Design & Analysis of VLSI Circuits, L. A. Glassey & D. W. Dobbepahl, Addison Wesley Pub Co. 1985. H. Bhatnagar, Advanced ASIC Chip Synthesis Using Synopsys Design Compiler Physical Compiler and Prime Time, 2nd edition, 2001. Static Timing Analysis for Nano meter Designs A Practical Approach, J. Bhasker • Rakesh Chadha, SpringerScience+Business Media, LLC 2009 Tools: Cadence Innovous, Encounter 	Standard data formats for repres	senting technology and design:	LEF, LIDERTY, SDC, DEF and SPEF.
 Chapter No. 5. Packaging An overview of package design and implementation and system level timing. Reference Books: The Design & Analysis of VLSI Circuits, L. A. Glassey & D. W. Dobbepahl, Addison Wesley Pub Co. 1985. H. Bhatnagar, Advanced ASIC Chip Synthesis Using Synopsys Design Compiler Physical Compiler and Prime Time, 2nd edition, 2001. Static Timing Analysis for Nano meter Designs A Practical Approach, J. Bhasker • Rakesh Chadha, SpringerScience+Business Media, LLC 2009 Tools: Cadence Innovous, Encounter 	Clock gating and power gating for reduction of device power consumption. Design for reliability:		
 An overview of package design and implementation and system level timing. Reference Books: The Design & Analysis of VLSI Circuits, L. A. Glassey & D. W. Dobbepahl, Addison Wesley Pub Co. 1985. H. Bhatnagar, Advanced ASIC Chip Synthesis Using Synopsys Design Compiler Physical Compiler and Prime Time, 2nd edition, 2001. Static Timing Analysis for Nano meter Designs A Practical Approach, J. Bhasker • Rakesh Chadha, SpringerScience+Business Media, LLC 2009 Tools: Cadence Innovous, Encounter 	Chapter No. E. Backaging		
 Reference Books: The Design & Analysis of VLSI Circuits, L. A. Glassey & D. W. Dobbepahl, Addison Wesley Pub Co. 1985. H. Bhatnagar, Advanced ASIC Chip Synthesis Using Synopsys Design Compiler Physical Compiler and Prime Time, 2nd edition, 2001. Static Timing Analysis for Nano meter Designs A Practical Approach, J. Bhasker • Rakesh Chadha, SpringerScience+Business Media, LLC 2009 Tools: Cadence Innovous, Encounter 	Chapter No. 5. Packaging		
 The Design & Analysis of VLSI Circuits, L. A. Glassey & D. W. Dobbepahl, Addison Wesley Pub Co. 1985. H. Bhatnagar, Advanced ASIC Chip Synthesis Using Synopsys Design Compiler Physical Compiler and Prime Time, 2nd edition, 2001. Static Timing Analysis for Nano meter Designs A Practical Approach, J. Bhasker • Rakesh Chadha, SpringerScience+Business Media, LLC 2009 Tools: Cadence Innovous, Encounter 	Perference Dealer		
 The Design & Analysis of VLSF circuits, L. A. Glassey & D. W. Dobbepani, Addison Wesley Pub Co. 1985. H. Bhatnagar, Advanced ASIC Chip Synthesis Using Synopsys Design Compiler Physical Compiler and Prime Time, 2nd edition, 2001. Static Timing Analysis for Nano meter Designs A Practical Approach, J. Bhasker • Rakesh Chadha, SpringerScience+Business Media, LLC 2009 Tools: Cadence Innovous, Encounter 	Reference DOURS:		
 Pub Co. 1985. H. Bhatnagar, Advanced ASIC Chip Synthesis Using Synopsys Design Compiler Physical Compiler and Prime Time, 2nd edition, 2001. Static Timing Analysis for Nano meter Designs A Practical Approach, J. Bhasker • Rakesh Chadha, SpringerScience+Business Media, LLC 2009 Tools: Cadence Innovous, Encounter 	1. The Design & Analysis of VESI Circuits, E. A. Glassey & D. W. Dobbepani, Addison Wesley		
 H. Bhatnagar, Advanced ASIC Chip Synthesis Using Synopsys Design Compiler Physical Compiler and Prime Time, 2nd edition, 2001. Static Timing Analysis for Nano meter Designs A Practical Approach, J. Bhasker • Rakesh Chadha, SpringerScience+Business Media, LLC 2009 Tools: Cadence Innovous, Encounter 	Pub Co. 1985.		
 Compiler and Prime Time, 2nd edition, 2001. 3. Static Timing Analysis for Nano meter Designs A Practical Approach, J. Bhasker • Rakesh Chadha, SpringerScience+Business Media, LLC 2009 Tools: Cadence Innovous, Encounter 	2. H. Bhatnagar, Advanced ASIC Chip Synthesis Using Synopsys Design Compiler Physical		
 Static Timing Analysis for Nano meter Designs A Practical Approach, J. Bhasker • Rakesh Chadha, SpringerScience+Business Media, LLC 2009 Tools: Cadence Innovous, Encounter 	Compiler and Prime Time, 2nd edition, 2001.		
Chadha, SpringerScience+Business Media, LLC 2009 Tools: Cadence Innovous, Encounter	3. Static Timing Analysis for Nano meter Designs A Practical Approach, J. Bhasker • Rakesh		
Tools: Cadence Innovous, Encounter	Chadha, SpringerScience+Business Media, LLC 2009		
Iools: Cadence Innovous, Encounter			



Program: Electronics & Communication Engineering		Semester: VII
Course Title: Microwave & Antenna		Course Code: 23EECE411
L-T-P: 3-0-0	Credits: 3	Contact Hours:3 hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 40Hrs	Examination Duration: 3 Hrs	

Chapter No. 1. Microwave Vacuum Tube Devices

Introduction, Reflex Klystron, Problems.

Chapter No. 2. Microwave Network Theory & Passive Devices

Introduction, S- Matrix Representation of Multiport network, Microwave Passive Devices: Directional couplers, Circulators, Magic T, Isolator, Attenuators, Numerical. Microwave Applications: Microwave Radar systems, microwave communication system, industrial applications of microwave: Microwave heating, thickness and moisture content measurement.

Unit II

Chapter No. 3. Antenna Parameters

Introduction, Basic antenna parameters ,Pattern, Beam width, Radiation intensity, Beam efficiency, Directivity, Gain, Aperture, Effective height, Polarization, Antenna field zone, The radio communication link. Radiation resistance of Short electric dipole and half wave length antenna.

Chapter No. 4. Sources and Arrays

Introduction, Point sources, Power patterns, Power theorem, Examples on power theorem, Directivity and beam width of point sources, Arrays of two isotropic point sources, Non isotropic but similar point sources and Pattern multiplication, Linear array of n isotropic point sources of equal amplitude and spacing, Broad side array, End fire array.

Unit III

Chapter No. 5. Antenna practice

Yagi-Uda Antenna, Dipole/Monopole antenna, Loop antenna, Horn antenna, Parabolic reflector, Helical antenna, Log periodic antenna, Microstrip Patch Antenna, Mobile Station Antennas, Antennas for GPR: Pulse Bandwidth, Embedded Antennas, UWB Antennas for Digital Applications, The Plasma Antenna, Types of antenna for 4G/LTE and 5G.

Text Book (List of books as mentioned in the approved syllabus)

- 1. PAnnapurna Das, Sisir K Das, Microwave engineering, TMH Publications, 2001.
- 2. J.D. Kraus & Khan, Antennas, third edition, MGH publication, 2006.
- 3. Liao, Microwave Devices and Circuits, PHI Pearson Education.

References

- 1. John Krauss and Daniel, Electromagnetics with Applications, 5th, McGraw-Hill, 1999.
- 2. E. C. Jordan, Electromagnetic waves & radiating systems, second edition, PHI publication.
- 3. K. D. Prasad, "Antenna and wave propagation" first edition, 1990.
- 4. C. A. Blains "Antenna theory and analysis and design", third edition, 1999.



Program: Electronics & Communication Engineering		Semester: VII
Course Title: AUTOSAR		Course Code: 20EECE406
L-T-P: 3-0-0	Credits: 3	Contact Hours:3 hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 40Hrs Examination Duration: 3 Hrs		

Chapter No. 1: AUTOSAR Fundamentals

Evolution of AUTOSAR – Motivations and Objectives AUTOSAR consortium – Stake holders – work Packages, AUTOSAR Partnership, Goals of the partnership, Organization of the partnership, AUTOSAR specification, AUTOSAR Current development status, BSW Conformance classes: ICC1, ICC2, ICC3, and Drawbacks of AUTOSAR.

Chapter No. 2: AUTOSAR layered Architecture

AUTOSAR Basic software, Details on the various layers, Details on the stacks Virtual Function Bus (VFB) Concept Overview of AUTOSAR Methodology, Tools and Technologies for AUTOSAR AUTOSAR Application Software Component (SW-C), Types of SW-components AUTOSAR Run Time Environment (RTE): RTE Generation Process: Contract Phase, Generation Phase, MCAL, IO HW Abstraction Layer, Partial Networking, Multicore, J1939 Overview, AUTOSAR Ethernet, AUTOSAR E2E Overview, AUTOSAR XCP, Metamodel, From the model to the process, Software development process.

Chapter No. 3: Methodology of AUTOSAR and Communication in AUTOSAR

CAN Communication, CAN FD, CANape, Application Layer and RTE, intra and inter ECU communication, Client-Server Communication, Sender-Receiver, Communication, CAN Driver, Communication Manager (ComM), Overview of Diagnostics Event and Communication Manager

Chapter No. 4: Overview about BSW constituents

BSW Constituents: Memory layer, COM and Services layer, ECU abstraction, AUTOSAR, Operating system, Interfaces: Standard interface, AUTOSAR standardized interface, BSW-RTE interface, (AUTOSAR interface), BSW-ECU hardware interface, Complex device drivers and BSW module configuration, AUTOSAR Integration.

Chapter 5: MCAL and ECU abstraction Layer

Microcontroller Drivers, Memory drivers: on-chip and off chip drivers, IO drivers(ADC, PWM, DIO), Communication drivers: CAN driver, LIN drivers, Flexrfay

Chapter 6: Service Layer

Diagnostic Event Manager, Function inhibits Manager, Diagnostic communication manager, Network management, Protocol data unit router, Diagnostic log and trace unit, COMM manager.

Text Book (List of books as mentioned in the approved syllabus)

1. Ronald K. Jurgen, Infotainment systems, 2007, SAE International, 2007 Back to Elective



Program: Electronics & Commur	nication Engineering	Semester: VII	
Course Title: Human Machine Interface		Course Code: 23EECE428	
L-T-P: 2-0-1	Credits: 3	Contact Hours:4 hrs/week	
ISA Marks: 100	ESA Marks:	Total Marks: 100	
Teaching Hours: 30Hrs	Examination Duration: 3 Hrs		
Unit I			
Chapter 1: Introduction to HMI			
Overview of HMI, general intr	oduction to HMI, HMI Archit	ecture & Concepts/HMI Sub-	
Components (Widgets, Framewo	ork, state machine)		
Chapter 2:Automotive HMI			
Evolution of HMI in cars, HMI for	car multimedia, GUI Tools (GTK	, QT, HTML5)	
Lab: Widget design using GUI too	bls		
Chapter 3:UX and Guidelines			
Introduction to UX design (theo	ory, design thinking), graphics o	design (Blender, GIMP), 2D/3D	
rendering, OpenGL, GPU archited	ctures, shader programming		
Lab: UX design using OpenGL, re	ndering using Blender.		
Unit II			
Chapter 4:Car Multimedia			
Instrument cluster, in-vehicle info	otainment, professional system/	rear-seat entertainment.	
Lab: Design instrument cluster fo	or dashboard and infotainment c	ontrol	
Chapter 5: App Development and	d Testing		
App development for Android/ iOS, Unity, HMI testing and automation Lab/ Project: Design an			
app to control vehicle infotainme	ent system using a mobile device		
Chapter 6: Advanced Topics			
Voice/ Gesture control, haptics, eye gaze sensor, Virtual/ Augmented Reality, Analytics			
References:			
1. The Handbook of Huma	1. The Handbook of Human-Machine Interaction: A Human-Centered Design Approach.		
Eds. G. A. Boy, CRC Press	Eds. G. A. Boy, CRC Press.		
2. Designing for Situation Av	wareness: An Approach to User-	Centered Design. M. R. Endsley	
& D. G. Jones, CRC Press.			
3. The Humane Interface	New Directions for Designing	Interactive Systems, I. Raskin	
Addison-Wesley			
Autoriale factoriale (11)	Plandar CIMP CTV OT		
4. Tutorials for tools/ librari	es: Blender, GIMP, GTK, QT, uni	ty, OpenGL	



Program: Electronics & Communication Engineering		Semester: VII
Course Title: Wireless & Mobile Communication		Course Code: 24EECE432
L-T-P: 3-0-0	Credits: 3	Contact Hours:3 hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 40Hrs	Examination Duration: 3 Hrs	

Chapter 01: Radio Propagation

Free space propagation model, Relating power to electric field., Relation, ground reflection, scattering, Practical link budget design using path loss model, Outdoor propagation models, Signal penetration into buildings, Ray tracking and site specific modelling, Small scale Multipath measurements, Parameters of mobile Multipath channels, Types of small scale fading.

Unit II

Chapter 02: Diversity techniques

Concept of Diversity branch and signal paths, Combining and switching methods, C/N, C/I performance improvements, RAKE receiver.

Chapter 03: Cellular concept

Frequency reuse, Channel assignment strategies, Handoff strategies, Interference and system capacity, Trucking and grade of service, Improving coverage, Capacity in cellular systems, FDMA, TDMA, Pseudo noise sequences, notion of spread spectrum, processing gain and Jamming margin, direct sequence spread spectrum, frequency hop spread spectrum, Spread spectrum multiple access, SDMA packet radio. Capacity of cellular systems.

Unit III

Chapter 4: 5G: Implementation, components of the 5G, 5G architecture, 5G design, 5G network, 5G applications, Advantages and disadvantages

Chapter 5: Satellite orbits GEO, MEO, LEO and applications.Fiber to the home (FTTH): Working, FTTH architecture and components, benefits, advantages and disadvantages

Text Book (List of books as mentioned in the approved syllabus)

1. T.S. Rapport, Wireless Communication, 2, Pearson Education, 2002

References

- 1. Kamil O Feher, Wireless digital communications: Modulation and spread spectrum Techniques, Prentice Hall of India, 2004
- 2. Vijay K Garg, IS_95 CDMA and cdma 2000, Pearson publication pvt. Ltd, 2004

3. Xiaodong Wang and Vincent Poor, wireless Communicating system: Advanced Techniques for signal Reception, Pearson publication pvt. Ltd, 2004



Program:Bachelor of Engineering (Electronics & Communication Engineering)	
Course Title::5G & Software Defined Networking	
Credits:: 3	Contact Hours: 4 hrs/week
ESA Marks:20	Total Marks:100
Examination Duration: :3Hrs	
	g (Electronics & ined Networking Credits:: 3 ESA Marks:20 Examination Duration: :3Hrs

Chapter No. 1: Overview of 5G Technology

Introduction to 5G NR and its importance in wireless communication Evolution from previous generations (1G to 4G) and key differences Use cases and applications of 5G technology Overview of 5G architecture and protocol stack Exploring NS-3 (Network Simulator 3) for code development

Chapter No. 2. Physical Layer Design and Techniques

Physical layer in 5G NR, waveforms, numerology, and frame structure Understanding modulation, coding, and MIMO techniques in 5G NR Hands-on exercises on simulating and implementing physical layer techniques using C/NS-3

- Simulating Basic NR Waveforms
- Implementing 5G NR Frame Structure
- Coding and Decoding Techniques in 5G NR

Chapter No. 3. Protocol Stack and Radio Access Network (RAN)

Overview of the protocol stack layers in 5G NR, including PHY, MAC, RLC, PDCP, and RRC. Understanding the functions and interactions between different protocol layers.5G RAN architecture, including gNBs (Next-Generation NodeBs) and NG-RAN interfaces

- Implementing Basic NR Physical Layer Procedures
- Designing a Simple NR MAC Scheduler
- Implementing RLC Layer Functionality for Data Segmentation and Reassembly
- Developing PDCP Layer for Header Compression and Encryption
- Establishing RRC Connection Setup and Management

Unit II

Chapter No. 4. Core Network Protocols and Technologies

Exploration of core protocols and technologies in 5G NR, including core network architecture, network slicing, and service-based architecture (SBA)

Implementation of key core network protocols using software-defined networking (SDN) principles and open-source tools

- Simulating Basic Network Functionality in 5G Core
- Implementing Authentication and Security Mechanisms
- Setup of Basic Session Management in 5G Core

Chapter No. 5. Network Slicing, Quality of Service (QoS), and Emerging Trends

Understanding network slicing concepts and its role in enabling customized services in 5G NR Implementation of network slicing and QoS management using SDN principles and open-source software platforms

Overview of emerging technologies beyond 5G NR, research challenges, and opportunities



Unit III

Chapter No. 6. Software-Defined Networking and Virtualization

OpenFlow Concepts :Match fields and actions in OpenFlow protocol Flow tables and pipeline stages in OpenFlow switches

SDN Controllers :Centralized, distributed, and hybrid SDN controller architectures Overview of popular SDN controllers: Open Daylight, ONOS, Ryu, Floodlight

SDN Applications :Traffic engineering and load balancing in SDN networks Network slicing and virtualization for resource allocation

Programmable Data Planes : Overview of programmable data plane technologies such as P4 Benefits and challenges of programmable data planes in SDN

Network Function Virtualization (NFV) :Introduction to NFV and its relationship with SDN NFV orchestration and service chaining for network services

Text Books

- 1. "5G NR: The Next Generation Wireless Access Technology" by Erik Dahlman, Stefan Parkvall, Johan Sköld (Academic Press)
- "Software-Defined Networking: Anatomy of OpenFlow" by Flavio Esposito, William M. Jr. (O'Reilly Media)

Reference Books:

- 1. "5G Mobile Communications" by Mischa Dohler, Afif Osseiran (Wiley)
- 2. "Software Defined Networks: A Comprehensive Approach" by Paul Goransson, Chuck Black (Morgan Kaufmann)



Brogram:Bacholor of Engineerin	g (Electronics &	Somostor: VII
Communication Engineering		Semester. VII
Course Title:Product and Functional safety		Course Code:24EECE433
L-T-P: 3-0-0	Credits:3	Contact Hours:3 hrs/week
ISA Marks:50	ESA Marks:50	Total Marks:100
Teaching Hours:40Hrs	Examination Duration:3hrs	
Unit I		
Chapter 1: Introduction to Prod	uct Safety	
Introduction, What Is Safety?, P	roduct-Safety Management vers	us Product-Safety Engineering,
Product Safety and Product-Safe	ty Engineering, History and Safe	ty, Product Liability
Chapter 2: International Regulation	tions and Global Market Access	
Regional Regulations: How The	y Differ, CE Marking, NRTLs, Ce	ertification Body (CB) Scheme,
Product Certification Marks, ISO	Registration Process	
Chapter 3: Product Safety Stand	ards	
Introduction, Product Safety and	I Standardization, What Is a Stan	dard? Structure of the Product
Safety Standard, Conformity to	o Product Safety Standards, C	bjectives for Products Safety
Standards, Product Safety Standa	ard Developers.	
Chapter 4: Hazards, Risks, Accid	ents, and Outcomes	Assidents and Outsomers Disk
Introduction, Recent History of	System Salety, Hazards, Risks,	Accidents and Outcomes, Risk
Charter C. Exactional Sofety in I	DeedVahieles	
Introduction Quality Managem	Road venicies	tomotive and Safety life cycles
Hazard Analysis and Risk Assess	ment according to ISO 26262	Safety Goals Safety Concents
Product Development at System	and component Level Verification	ons and Tests Safety Validation
Approvals/Releases		
Unit III		
Chapter 5: Methods for Failure	Analysis	
Introduction to analysis, FMEA, I	TA, HAZOP, AEA	
Chapter 7: STPA, SOTIF and ISO		
Introduction to STPA, SOTIF, Integration with ISO		
Text Books		
1 "Engineering Ethics and		
	Design for Product Safety", 1st	Edition, ISBN: 9781260460537,
McGraw Hill.	Design for Product Safety", 1st	Edition, ISBN: 9781260460537,
McGraw Hill. 2. "Electrical product comp	Design for Product Safety", 1st liance and safety engineering", S	Edition, ISBN: 9781260460537, teli L., Constantin B., Jan Swart,
 McGraw Hill. 2. "Electrical product comp Artech House, 2017 	Design for Product Safety", 1st liance and safety engineering", S	Edition, ISBN: 9781260460537, teli L., Constantin B., Jan Swart,
 McGraw Hill. "Electrical product comp Artech House, 2017 "Functional Safety for Ro 	Design for Product Safety", 1st liance and safety engineering", S pad Vehicles New Challenges ar	Edition, ISBN: 9781260460537, teli L., Constantin B., Jan Swart, nd Solutions for E-mobility and
 Angineering Ethics and McGraw Hill. "Electrical product comp Artech House, 2017 "Functional Safety for Ro Automated Driving", Han 	Design for Product Safety", 1st liance and safety engineering", S pad Vehicles New Challenges ar s-Leo Ross, Springer Internation	Edition, ISBN: 9781260460537, teli L., Constantin B., Jan Swart, nd Solutions for E-mobility and al Publishing Switzerland 2016.
 Angineering Ethics and McGraw Hill. "Electrical product comp Artech House, 2017 "Functional Safety for Re Automated Driving", Han Reference Books: 	Design for Product Safety", 1st liance and safety engineering", S pad Vehicles New Challenges ar s-Leo Ross, Springer Internations	Edition, ISBN: 9781260460537, teli L., Constantin B., Jan Swart, nd Solutions for E-mobility and al Publishing Switzerland 2016.
 Anglicering Ethics and McGraw Hill. 2. "Electrical product comp Artech House, 2017 3. "Functional Safety for Ro Automated Driving", Han Reference Books: 1. "The Safety Critical System: 	Design for Product Safety", 1st liance and safety engineering", S bad Vehicles New Challenges ar s-Leo Ross, Springer Internations	Edition, ISBN: 9781260460537, teli L., Constantin B., Jan Swart, nd Solutions for E-mobility and al Publishing Switzerland 2016. Guide to Functional Safety: IEC

2. "Assessment of Safety Standards for Automotive Electronic Control Systems", Van Eikema Hommes, Qi D, National Highway Traffic Safety Administration



3. "Functional Safety: A Straightforward Guide to Applying IEC 61508 and Related Standards", David J. Smith and Kenneth G. L. Simpson.



Program: Bachelor of Engineering (Electronics &		Semester: VII
Communication Engineering)		
Course Title: GEN AI		Course Code:24EECE435
L-T-P: 2-0-1	Credits:3	Contact Hours:4 hrs/week
ISA Marks:80	ESA Marks:20	Total Marks:100
Teaching Hours:40Hrs	Examination Duration:3hrs	

Chapter 1: Introduction to Generative AI

Definition, Overview of Generative AI, Importance and applications of Generative AI, Evolution of AI towards generative models, Key milestones and breakthroughs in Generative AI.

Chapter 2: Generative Models I:

Autoencoders (AE) and Variational Autoencoders (VAEs) Architecture: Encoder, Decoder, Latent Space, Training with ELBO (Evidence Lower Bound), Applications and limitations.

Generative Adversarial Networks (GANs): Architecture: Generator and Discriminator, Training process, loss functions, Common issues, Variants: DCGAN, Cycle GAN, and Style GAN.

Diffusion Models: Forward process (encoders), reverse process (decoders), score matching, guided diffusion

Chapter 3: Training and Evaluation of Generative AI Models:

<u>Optimization Methods</u>: Gradient Descent, Stochastic Gradient Descent (SGD), Adam Optimizer, Adam (Adaptive Moment Estimation), RMS Prop (Root Mean Square Propagation), Ada grad (Adaptive Gradient Algorithm), Ada Delta.

<u>Evaluation Metrics:</u> Inception Score (IS), Freshet Inception Distance (FID), Perplexity, Reconstruction Error, Mode Score, Diversity Metrics, Wasserstein Distance, Earth Mover's Distance (EMD), BLEU Score

Challenges: Mode collapse, stability, and convergence.

Unit II

Chapter 4: Generative Models II: Autoregressive Models

Definition and Principle: Autoregressive Property, Conditional Dependence, Autoregressive Process Examples of Autoregressive Models: AR Models in Time Series Analysis, Autoregressive Integrated Moving Average (ARIMA) Autoregressive Models for Generative AI: Pixel CNN - Overview, Architecture, Training, Applications Wave Net - Overview, Architecture, Training, Applications

Chapter 5: Generative Models II: Transformers

Introduction to Transformers, Origins and evolution from traditional sequence models (like RNNs and LSTMs) to transformers, self-attention mechanism, multi-head attention, position wise feedforward networks. Transformer Architecture: breakdown of encoder and decoder stacks, Layer normalization and residual connections, Masked self-attention in the decoder for auto-regressive generation, Pre-training and Fine-tuning. Transformer-based Autoregressive Models: Overview, Architecture, Training, Applications, BERT (Bidirectional Encoder Representations from Transformers), T5 (Text-to-Text Transfer Transformer)

Chapter 6: Generative Models II: Large Language Models (LLMs)

Introduction to LLMs, Overview of Large Language Models (e.g., GPT-3, GPT-4), Training methodologies and scalability, Integration of LLMs in various generative tasks, Fine-tuning and transfer learning with LLMs, Building and deploying LLM-based applications.

Unit III

Chapter 7: Advanced Topics in Generative AI:



Flow-Based Models, Invertibility, Volume Preservation, Normalizing Flows, Invertible Convolution, Coupling Layers Sparse Attention Mechanisms, Multimodal Generative Models, Meta-Learning and Few-Shot Learning, Continual Learning and Transfer Learning, Privacy-Preserving Generative Models, Quantum Generative Models

Chapter 8: Ethical Considerations and Responsible AI:

Bias and fairness in generative AI models, Privacy concerns and data protection in generative AI applications, Responsible use of generative models in society

KLE Technological University Creating Value, Leveraging Knowledge

Program: Bachelor of Engineerin	ng (Electronics &	Semester: VII
Communication Engineering)		
Course Title: Advance IC Packaging		Course Code:24EECE436
L-T-P: 2-0-1	Credits:3	Contact Hours:4 hrs/week
ISA Marks:100	ESA Marks:	Total Marks:100
Teaching Hours:40Hrs	Examination Duration:3hrs	
Chapter 1: Introduction to Adva	nced Semiconductor Packaging	
Overview of semiconduct	or packaging	
Evolution of packaging te	chnologies	
Challenges and trends in	advanced packaging	
Chapter 2: Packaging Materials	and Processes	
Materials used in advance	ed packaging	
 Assembly and packaging 	processes	
 Flip-chip, wafer-level pac 	kaging, and 3D packaging	
Thermal and reliability co	nsiderations	
Chapter 3: System-in-Package (S	iP) and Multi-Chip Modules (M	CM)
 Introduction to SiP and N 	ICM	
Design considerations for SiP and MCM		
 Introduction to SerDes, on-die PHYs and signal integrity 		
Chapter 4: Advanced Interconne	ect Technologies	
 Micro bump and fine-pito 	ch technologies	
 Through-Silicon Via (TSV) 	and 3D interconnects	
High-density interconnec	 High-density interconnects (HDI) 	
	. ,	
Chapter 5: Layout of Package Su	bstrates (Lecture & Lab)	
 Review provided bump-to 	p-ball connectivity data and fill c	out assigned lab worksheet
 Open single-die package 	layout database in a commerci	al package design tool such as
APD+ and explore signal r	outing and power planes, filling	out assigned lab worksheet
Given a bump-to-ball map and substrate layer information, implement substrate layout		
Chapter 6: Lavout of Silicon Interposers (Lecture & Lab)		
Layout a silicon interpose	r given a micro bump map for a	n ASIC and C4 ball assignments
using a commercial route	r such as In Novus	Ŭ
Deference Deele		
1. Kao K Tummala, Fundam	entals of Device and Systems Pa	ckaging, McGraw Hill, 2020.

- 2. Glenn R. Blackwell, The Electronics Packaging Handbook, CRC Press, 2017.
- 3. Bernard S Matisoff, Handbook of Electronics Packaging Design and Engineering, Springer, 2012.
- 4. Rao R Tummala, Fundamentals of Microsystems Packaging, McGraw Hill, 2001.



Program: Bachelor of Engineering (Electronics & Communication Engineering)		Semester: VIII
Course Title: OOPS using C++		Course Code:23EECE421
L-T-P: 2-0-1	Credits:3	Contact Hours: 4 hrs/week
ISA Marks:100	ESA Marks:	Total Marks:100
Teaching Hours:30Hrs	Examination Duration:3Hrs	

UNIT I

Chapter 1: Fundamental concepts of object oriented programming:

Introduction to object oriented programming, Programming Basics (keywords, identifiers, variables, operators, classes, objects), Arrays and Strings Functions/ methods (parameter passing techniques)

Chapter 2: OOPs Concepts:

Overview of OOPs Principles, Introduction to classes & objects, Creation & destruction of objects, Data Members, Member Functions, Constructor & Destructor, Static class member, Friend class and functions, Namespace

UNIT II

Chapter 3: Inheritance:

Introduction and benefits, Abstract class, Aggregation: classes within classes, Access Specifier, Base and Derived class Constructors, Types of Inheritance, Function overriding

Chapter 4: Polymorphism:

Virtual functions, Friend functions, static functions, this pointer

Unit III

Chapter 5: Exception Handling:

Introduction to Exception, Benefits of Exception handling, Try and catch block, Throw statement, Pre-defined exceptions in C++, Writing custom Exception class

Chapter 6: I/O Streams:

C++ Class Hierarchy, File Stream, Text File Handling, Binary File Handling Error handling during file operations, Overloading << and >> operators

Textbook:

1. Robert Lafore, "Object oriented programming in C++", 4th Edition, Pearson education, 2009. Neural Networks and Deep Learning by Michael Nielsen.

Reference books:

- 1. Lippman S B, Lajorie J, Moo B E, C++ Primer, 5ed, Addison Wesley, 2013.
- 2. Herbert Schildt: The Complete Reference C++, 4th Edition, Tata McGraw Hill



Program: Bachelor of Engineering (Electronics & Communication Engineering)		Semester: VII
Course Title: Phase-locked loops(Swayam)		Course Code:22EECE432
L-T-P: 0-0-3	Credits:3	Contact Hours:6 hrs/week
ISA Marks:100	ESA Marks:	Total Marks:100
Teaching Hours:42Hrs	Examination Duration:3Hrs	
Pack to Elective		

Back to Elective

Program: Bachelor of Engineering (Electronics &		Semester: VII
Communication Engineering)		
Course Title: VLSI Design Flow: RTL to GDS (Swayam)		Course Code:23EECE435
L-T-P: 0-0-3	Credits:3	Contact Hours:6 hrs/week
ISA Marks:100	ESA Marks:	Total Marks:100
Teaching Hours:42Hrs	Examination Duration:3Hrs	
Back to Elective		

Back to Elective

Program: Bachelor of Engineering (Electronics & Communication Engineering)		Semester: VII
Course Title: Cyber Security and Privacy (Swayam)		Course Code:23EECE439
L-T-P: 0-0-3	Credits:3	Contact Hours:6 hrs/week
ISA Marks:100	ESA Marks:	Total Marks:100
Teaching Hours:42Hrs	Examination Duration:3Hrs	

Program: Bachelor of Engineering (Electronics & Communication Engineering)		Semester: VII
Course Title: Introduction To Algorithms And Analysis (Swayam)		Course Code:23EECE440
L-T-P: 0-0-3 Credits:3		Contact Hours:6 hrs/week
ISA Marks:100 ESA Marks:		Total Marks:100
Teaching Hours:42Hrs Examination Duration:3Hrs		
Back to Elective		



Program: Bachelor of Engineering (Electronics & Communication Engineering)		Semester: VII
Course Title: Introduction to Internet of Things(Swayam)		Course Code:24EECE446
L-T-P: 0-0-3	Credits:3	Contact Hours:6 hrs/week
ISA Marks:100	ESA Marks:	Total Marks:100
Teaching Hours:42Hrs	Examination Duration:3Hrs	



Program: Bachelor of Engineering (Electronics &		Semester: VIII
Communication Engineering)		
Course Title: Introduction to Deep Learning		Course Code:23EECE422
L-T-P: 2-0-1	Credits:3	Contact Hours: 4 hrs/week
ISA Marks:80	ESA Marks:20	Total Marks:100
Teaching Hours:30Hrs	Examination Duration:3Hrs	

Chapter 1: Introduction to Deep Learning

What is Deep Learning?, Applications of deep learning, Differences between machine learning and deep learning, Basics of Neural Networks, Supervised Learning with Neural Networks, Logistic regression as a neural network, Computation graph, shallow neural networks, Deep neural networks

Chapter 2: Hyper-Parameter Tuning, Regularization and Optimization

Basics of Hyper-parameters, Regularization, Need for regularization, dropout regularization, gradient checking, mini-batch gradient descent, exponentially weighted averages and its bias correction, Gradient descent with decay, Adam's optimization algorithm, The problem of local minima, weight initialization in neural networks, Normalizing activations in a network, Fitting Batch norm into a network, Softmax regression, Softmax classifier, Introduction to metric tensors and tensorflow, Basic programs in tensorflow.

Unit II

Chapter 3: Convolutional Neural Networks

Introduction to Computer Vision and Image Processing, 2D Convolutions, Strided convolution, convolution over volume, One layer of a convolution network, ReLu and pooling, Example of a ConvNet, Classic CNN Networks, ResNet architecture, Inception Networks, Transfer learning, Data Augmentation, Basics of Keras, Residual networks, Object Localization, Landmark and object detection, Convolutional implementation of sliding windows, YOLO algorithm, Car detection algorithm using YOLO, One shot learning, Face recognition algorithm.

Chapter 4: Recurrent Neural Networks

Back propagation through time, RNN model, Types of RNN, Vanishing gradients with RNN, Gated Recurrent Unit, LSTM, Bidirectional RNN, Deep RNN, basics of NLP and Concept of word embedding, speech recognition.

Unit III

Chapter 5: Unsupervised Deep Learning

Concepts of Unsupervised deep learning, RBM (Restricted Boltzman Machine) and auto encoders, structure of Auto encoders, collaborative filtering with RBM, Deep belief networks.

Textbook:

- 1. Deep Learning, Ian Goodfellow and Yoshua Bengio and Aaron Courville, MIT Press, http://www.deeplearningbook.org, 2016.
- 2. Neural Networks and Deep Learning by Michael Nielsen.



Reference books:

- 1. Deep Learning with Python, Francois Chollet, by Manning Publications, 2018.
- 2. Deep Learning by Microsoft Research
- 3. Deep Learning Tutorial by LISA lab, University of Montreal



Program: Bachelor of Engineering (Electronics &		Semester: VIII
Communication Engineering)		
Course Title: Digital Image Processing		Course Code:23EECE414
L-T-P: 2-0-1	Credits:3	Contact Hours:4 hrs/week
ISA Marks:80	ESA Marks:20	Total Marks:100
Teaching Hours:30Hrs	Examination Duration:3Hrs	

Chapter 1. Introduction

Introduction to Image processing and Computer Vision. Application domains of Image processing and computer vision. Image acquisition, sampling, quantization, temporal properties of vision.

Chapter 2. Image Formation

Fundamental Concepts of Image Formation: Radiometry, Geometric Transformations, Geometric Camera Models. Camera Calibration, Image Formation in a Stereo Vision Setup, Image Reconstruction from a Series of Projections

Unit II

Chapter 3. Image Transforms

2D orthogonal and unitary transforms, DFT, DCT, DST, KLT transforms

Chapter 4. Image Enhancement

Histograms modelling, spatial operations, transform operations, multispectral image enhancement

Chapter 5. Image Descriptors and Features

Texture Descriptors, Colour Features, Edges/Boundaries. Interest or Corner Point Detectors, Histogram of Oriented Gradients, Scale Invariant Feature Transform, Speeded up Robust Features, Saliency

Unit III

Chapter 6. Filtering and Restoration

Colour Image Processing, Image Segmentation, Image observation models, Inverse and wiener filtering

Textbook:

- 1. Rafael C. Gonzalez & Richard E. Woods, "Digital Image Processing", Third Edition, Pearson.
- 2. NOC | Computer Vision and Image Processing Fundamentals and Applications (nptel.ac.in)

Reference books:

```
1. A.K. Jain, "Fundamentals of Digital Image Processing", Pearson Education (Asia) Pvt. Ltd.
```



Program: Electronics & Communication Engineering		Semester: VIII
Course Title: MEMS		Course Code: 23EECE403
L-T-P: 2-0-1	Credits: 3	Contact Hours: 4 hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 30Hrs	Examination Duration: 3 Hrs	
Unit I		
Overview of MEMS and Microsystems Evolution of Microsystems, Miniaturization, Applications of Microsystems in Automotive,		
Aerospace, Health Care Industry, Industrial Products, Consumer Products and Telecommunications.		
Working principles of Microsyste	ems	
Micro-sensors: Acoustic wave s	ensor, Biomedical Sensors and	Biosensors, Chemical Sensors
Optical Sensors, Pressure Sensor	s, Thermal Sensors.	
Micro-actuation: Actuation Usin	g Thermal Forces, Shape Mem	ory Alloys (SMA), Piezoelectric
Crystals and Electrostatic Forces.		
Applications of Micro-actuations	: Micro-grippers, Micro-motors,	Micro-valves, Micro-pumps.
Scaling laws in miniaturization Introduction to scaling, Scaling Electromagnetic Forces, Electricit Materials for MEMS and Microso Substrate and Wafers, Active Compounds, Silicon Piezo resisto Packaging Materials. Unit III Microsystems Fabrication Proces Photolithography, Ion Implantat Physical Vapor Deposition (PVD), Micro manufacturing: Bulk Micro Text Book:	g in Geometry, Rigid-Body D ty, Fluid Mechanics, Heat Transfe ystem Substrate Materials, Silicon a ors, Gallium Arsenide, Quartz, P sses cion, Diffusion, Oxidation, Cher Etching.	ynamics, Electrostatic Forces, er, Numerical problems. as Substrate Material, Silicon Piezoelectric Crystals, Polymers, mical Vapor Deposition (CVD), omachining, The LIGA Process.
1. "MEMS and Microsystem	s– Design and Manufacture", Ta	i-Ran Hsu, TMH Edition 2002.
References:		
1. "Micro system Design", Stephen D. Senturia, Kluwer Academic Publishers, 2001.		
2. "Foundations of MEMS", Chang Liu, Pearson Edition 2012.		
 "RF MEMS:Theory, Desi Publication, 2003. 	gn, and Technology", Gabriel I	M. Rebeiz, John Wiley & Sons



Program: Electronics & Communication Engineering		Semester: VIII
Course Title: Automotive Electronics		Course Code: 18EECO403
L-T-P: 3-0-0	Credits: 3	Contact Hours: 3 hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 40Hrs	Examination Duration: 3 Hrs	

Chapter No: 1. Introduction to Vehicle Drivelines / Power train Systems

Overview of Automotive industry, ECU Design Cycle: Types of model development cycles (V and Agile), Components of ECU, Examples of ECU on Chassis, Infotainment, Body Electronics and cluster. Introduction to power train, manual and automatic transmissions, automotive axles, 4-wheel and 2-wheel drives, Vehicle braking fundamentals, Steering Control, Overview of Hybrid Vehicles,

Chapter No: 2. Automotive Control Systems Design

Derivation of models and design of control strategies for power train control modules and integration into automotive platforms. Engine control functions, Fuel control, Electronic systems in Engines, Development of control algorithm for EMS with consideration of vehicle performance. Automotive grade microcontrollers: Architectural attributes relevant to automotive applications, Automotive grade processors ex: Renesas, Quorivva, and Infineon.

Chapter No: 3. Automotive Sensors and Actuators

Sensor characteristics, Sensor response, Sensor error, Redundancy of sensors in ECUs, Avoiding redundancy, Smart Nodes, Examples of sensors: Accelerometer (knock sensors), wheel speed sensors, Engine speed sensor, Vehicle speed sensor, Throttle position sensor, Temperature sensor, Mass air flow (MAF) rate sensor, Exhaust gas oxygen concentration sensor, Throttle plate angular position sensor, Crankshaft angular position/RPM sensor, Manifold Absolute Pressure (MAP) sensor. Actuators: Engine Control Actuators, Solenoid actuator, Exhaust Gas Recirculation Actuator.

Unit II

Chapter No:4. Automotive Stability and Safety Systems

Passive/active safety systems and design philosophies. Investigation of stability issues associated with vehicle performance and the use of sensors and control system strategies for stability enhancement. Implementation and application to intelligent cruise control, lane departure warning systems, ABS, Traction Control, active steering systems, vehicle dynamic control systems.

Chapter No:5. Automotive communication protocols

Overview of Automotive communication protocols : CAN, CAN FD, SOME/ IP Protocol, LIN , Flex Ray, MOST

Unit III

Chapter No: 6. Overview of ADAS/AV and Functional safety standards

Advanced Driver Assistance Systems (ADAS), Autonomous vehicle basics, sensing, planning and controls for autonomous driving, connected vehicles.

Functional Safety: Need for safety standard-ISO 26262, safety concept, safety process for product life cycle, safety by design, validation.



Chapter No:7. Diagnostics and Reliability

Discussion of legislated state, federal and international requirements. On-board automotive sensors to monitor vehicle operation, typical diagnostic algorithms. Analytical methods for designing fault-tolerant systems and assessing vehicle reliability, including safety critical systems and 'limp-home' modes. Use of handheld scanners and specialized diagnostic equipment to classify faults. Diagnostic protocols: KWP2000 and UDS.

Text Books

- 1. Ribbens, Understanding of Automotive electronics, 8th edition, Elsevier, 2017
- 2. Denton.T, Automobile Electrical and Electronic Systems, 5th edition, Routledge, 2017
- 3. Denton.T, Advanced automotive fault diagnosis, 4th edition Routledge, 2016

Reference Books:

- 1. Ronald K Jurgen, Automotive Electronics Handbook, 2nd Edition, McGraw-Hill, 1999
- 2. JamesD Halderman, Automotive electricity and Electronics, 5th edition, Pearson, 2016
- 3. Allan Bonnick, Automotive Computer Controlled Systems Diagnostic Tools and Techniques, Elsevier Science, 2001
- 4. Nicholas Navet , Automotive Embedded System Handbook ,2009



Program: Electronics & Communication Engineering		Semester: VIII
Course Title: Project Work		Course Code: 20EECW402
L-T-P: 0-0-11	Credits: 11	Contact Hours: 22 hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours:	Examination Duration: 3 Hrs	
e Smart City		

- Smart City
 Connected Ca
- Connected Cars
 Home Automation
- Home Automatic
- Health care
- Smart energy
- Automation of Agriculture

Guide lines for selection of a project:

• The project needs to encompass the concepts learnt in the previous semesters, so that the student will learn to integrate, the knowledge base acquired to provide a solution to the defined problem statement of the project work.

- Student can select a project which leads to a product or model or prototype.
- Time plan: Effort to do the project should be between 60-70 Hrs per team, which includes self-study of an individual member (80-100 Hrs) and team work (40-50 hrs).
- Learning overhead should be 20-25% of total project development time.

Criteria for group formation:

- 3-4 students in a team.
- Role of teammates: Team lead and members.

Allocation of Guides and Mentors for the projects:

Every Project batch will be allocated with one faculty.

Details of the project batches:

- Number of faculty members: 50
- Number of students:3-4 students in a team.

Role of a Guide

The primary responsibility of the guide is to help students to understand the meaning and need of various stages in the implementation of the project. At every stage of the project development, guide should help towards its successful completion as per the predefined standards.

How student should carry out a project:

- Define the problem.
- Specify the requirements.
- Specify the design in the understandable form (Block Diagram, Flowchart, Algorithm, etc).
- Analyze the design and identify hardware and software components separately.
- Select appropriate simulation tool and development board for the design.
- Implement the design.


- Optimize the design and generate the results.
- Result representation and analysis.
- Prepare a document and presentation.

Report Writing

- The format for report writing should be downloaded from ftp://10.3.0.3/projects
- The report needs to be shown to guide and committee for each review.
- •

Evaluation Scheme

- Internal semester assessment (ISA)
- Evaluation is done based on the evaluation rubrics given in Table 1
- Project shall be reviewed and evaluated by the concerned Guide for 50% of the marks.
- Project shall be evaluated by the review committee for 50% of the marks.

Back to Semester VIII



Program: Electronics & Communication Engineering		Semester: VIII	
Course Title: Internship- Training		Course Code: 18EECI493	
L-T-P: 0-0-6	Credits: 6	Contact Hours: 12 hrs/week	
ISA Marks: 50	ESA Marks: 50	Total Marks: 100	
Teaching Hours:	Examination Duration: 3 Hrs		
Evaluation parameters for Internship Training			
Initiative and creativity			
 Adaptation capacity 			
 Commitment and perseverance 			
Independence	 Independence 		
 Handling supervisor's comments and development skills 			
 Time management 			
 Formulation goals, framework project 			
 Theoretical underpinning, use of literature 			
 Use of methods and processing data 			
 Reflection on results 			
 Conclusions and discussion 			
 Presentation skills 			
 Presentation skills 			

Back to Semester VIII



Program: Electronics & Communication Engineering		Semester: VIII	
Course Title: Internship- Project		Course Code: 20EECW494	
L-T-P: 0-0-11	Credits: 11	Contact Hours: 22 hrs/week	
ISA Marks: 50	ESA Marks: 50	Total Marks: 100	
Teaching Hours:	Examination Duration: 3 Hrs		
Evaluation parameters for Internship Project			
Initiative and creativity			
 Adaptation capacity 			
 Commitment and perseverance 			
 Independence 			
 Handling supervisor's comments and development skills 			
 Time management 			
 Formulation goals, framework project 			
 Theoretical underpinning, use of literature 			
 Use of methods and processing data 			
 Reflection on results 			
 Conclusions and discussion 			
 Presentation skills 			

Back to Semester VIII