KLE Technological University | Creating Value, Leveraging Knowledge

Curriculum Structure and Curriculum Content for the Academic Batch – 2022-26
School /Department: Electrical & Electronics Engineering
Program: Electronics Engineering (VLSI Design & Technology)

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Vision and Mission of KLE Technological University

Vision

KLE Technological University will be a national leader in Higher Education–recognised globally for innovative culture, outstanding student experience, research excellence and social impact.

Mission

KLE Technological University is dedicated to teaching that meets highest standards of excellence, generation and application of new knowledge through research and creative endeavors.

The three-fold mission of the University is:

- To offer undergraduate and post-graduate programs with engaged and experiential learning environment enriched by high quality instruction that prepares students to succeed in their lives and professional careers.

- To enable and grow disciplinary and inter-disciplinary areas of research that build on present strengths and future opportunities aligning with areas of national strategic importance and priority.

- To actively engage in the Socio-economic development of the region by contributing our expertise, experience and leadership, to enhance competitiveness and quality of life.

As a unified community of faculty, staff and students, we work together with the spirit of collaboration and partnership to accomplish our mission.

Vision and Mission Statements of the School / Department

Vision

KLE Tech-Department of Electronics Engineering (VLSI Design and Technology) will be well recognized nationally and internationally for excellence in its educational programs, pioneering research and impact on the industry and society.

Mission

- **Electronics Engineering (VLSI Design and Technology)** at KLE Tech prepares students to design the core of modern electronics—from semiconductor chips to intelligent systems. The program builds strong foundations in circuit design, digital systems, and VLSI, with emphasis on hardware-software integration.
- Students gain expertise in analog/digital IC design, RTL and physical design, verification, and system-level integration. The program also introduces advanced IC packaging technologies, including 2.5D/3D integration, chiplets, and System-in-Package (SiP), essential for high-performance and compact electronic systems.
- With specialized labs, industry-standard EDA tools, and project-based learning, the program makes students industry-ready for roles in domains such as mobile and edge computing, AI hardware, automotive electronics, medical electronics, IoT systems, and consumer smart devices.
- Soft skill development, coding proficiency, and exposure to research and innovation are embedded throughout the curriculum. Students graduate not just as engineers, but as solution creators driving the future of an intelligent, efficient, and connected world.

Program Educational Objectives/Program Outcomes and Program-Specific Objectives

Program Educational Objectives -PEO's
1. Graduates will demonstrate peer- recognized technical competency to solve contemporary problems in the analysis, design and development of electronic devices and systems.
2. Graduates will demonstrate leadership and initiative to advance professional and organizational goals with commitment to ethical standards of profession, teamwork and respect for diverse cultural background.
3. Graduates will be engaged in ongoing learning and professional development through pursuing higher education, and self-study.
4. Graduates will be committed to creative practice of engineering and other professions in a responsible manner contributing to the socio-economic development of the society.
Program Outcomes-PO's
PO1:Engineering knowledge: Apply knowledge of mathematics, natural science, computing, engineering fundamentals and an engineering specialization as specified in WK1 to WK4 respectively to develop to the solution of complex engineering problems.
PO 2: Problem analysis: Identify, formulate, review research literature and analyze complex engineering problems reaching substantiated conclusions with consideration for sustainable development. (WK1 to WK4)
PO 3:Design/Development of Solutions: Design creative solutions for complex engineering problems and design/develop systems/components/processes to meet identified needs with consideration for the public health and safety, whole-life cost, net zero carbon, culture, society and environment as required. (WK5)
PO4:Conduct investigations of complex problems: Conduct investigations of complex engineering problems using research-based knowledge including design of experiments, modelling, analysis & interpretation of data to provide valid conclusions. (WK8).
PO 5: Engineering Tool Usage: Create, select and apply appropriate techniques, resources and modern engineering & IT tools, including prediction and modelling recognizing their limitations to solve complex engineering problems. (WK2 and WK6)
PO 6: The Engineer and The World:

Analyze and evaluate societal and environmental aspects while solving complex engineering problems for its impact on sustainability with reference to economy, health, safety, legal framework, culture and environment. (WK1, WK5, and WK7).
PO 7: Ethics: Apply ethical principles and commit to professional ethics, human values, diversity and inclusion; adhere to national & international laws. (WK9)
PO 8: Individual and Collaborative Team work: Function effectively as an individual, and as a member or leader in diverse/multi-disciplinary teams.
PO 9:Communication: Communicate effectively and inclusively within the engineering community and society at large, such as being able to comprehend and write effective reports and design documentation, make effective presentations considering cultural, language, and learning differences
PO 10: Project management and finance: Apply knowledge and understanding of engineering management principles and economic decision-making and apply these to one's own work, as a member and leader in a team, and to manage projects and in multidisciplinary environments.
PO11:Life-long learning: Recognize the need for, and have the preparation and ability for i) independent and life-long learning ii) adaptability to new and emerging technologies and iii) critical thinking in the broadest context of technological change. (WK8)
Program Specific Objectives -PSO's
PSO 1: Ability to apply design principles in developing embedded systems, VLSI circuits, and software components for hardware-software solutions.
PSO 2: Demonstrate proficiency in using industry-standard EDA tools for front-end and back-end VLSI design, with exposure to advanced IC packaging technologies.

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Curriculum Structure-Overall

Semester								
	Total Program Credits: 180							
Course with course code	I	II	III	IV	V	VI	VII	VIII
	Single Variable Calculus 18EMAB101 4-1-0	Multivariable Calculus 18EMAB102 4-0-1	BS: Integral Transform and Statistics 15EMAB203 4-0-0	BS: Linear Algebra & Partial Differential Equations 15EMAB208 4-0-0	PC10: CMOS VLSI Design 24EVTC301 4-0-0	Physical Design Analog 24EVTC307 1-0-2	CMOS ASIC Design 25EVTC401 (1-0-2)	PSE Elective 6 (22EVTExxx) 3 credits
	Engineering Chemistry 15ECHB102 3-0-0	Engineering Physics 15EPHB101 3-0-0	ES1: Corporate Communication 22EHSH201 0.5-0-0	ES2: Problem Solving & Analysis 22EHSH202 0.5-0-0	PC11: Control System 24EVTC302 4-0-0	PC14: VLSI Fabrication Technology 24EVTC308 2-0-0	PSE Elective 2 (24EVTExxx) 3 credits	Open Elective 1 (22EVTExxx) 3 credits
	Engineering Mechanics 15ECVF101 4-0-0	Problem Solving wit Data Structures 18ECSP102 0-0-3	PC1: Circuit Analysis 23EVTC201 4-0-0	ES4: Semiconductor Device Physics 23EVTC205 3-0-0	PC12: Machine Learning & Deep Learning 24EVTC303 2-0-2	System Verilog for Verification 24EVTC309 1-0-2	PSE Elective 3 (24EVTExxx) 3 credits	Project Work 25EVTW402 0-0-11
	C Programming for Problem solving 18ECSP101 0-0-3	Engineering Exploration 15ECRP101 0-0-3	PC2: Analog Electronic Circuits 23EVTC202 4-0-0	PC5: Linear Integrated Circuits 23EVTC206 4-0-0	PC13: Electromagnet Fields and Waves 24EVTC304 3-0-0	PSE Elective 1 (24EVTExxx) 3 credits	PSE Elective 4 (22EVTExxx) 3 credits	Internship- Training 24EVTI493 0-0-6 Internship- Project 24EVTW494 0-0-11
	Basic Electrical Engineering 18EEEF101 3-0-0	Basic Electronics 18EECF101 4-0-0	PC3: Digital Circuits 23EVTC203 4-0-0	PC6: Computer Architecture 23EVTC207 2-0-1	Digital Signal Processing and Architecture 24EVTC305 3-0-0	P2: Minor Project 24EVTW302 0-0-6	PSE Elective 4 (24EVTExxx) 3 credits	
	Design Thinking for Social Innovation 20EHSP101 0-1-1	Basic Mechanical Engineering 15EMEF101 2-1-0	PC4: Signals & System 23EVTC204 4-0-0	PC7: ARM Processor & Applications 23EVTC210 3-0-1	Analog Integrated Circuit Design 24EVTC306 2-0-1	GEN AI 24EVTC310 2-0-1	PSE Elective 5 (24EVTExxx) 3 credits	

	Professional Communication 15EHSH101 1-1-0	Applied Physics Lab 16EPHP101 0-0-1	PCL1: Digital Circuits Lab 23EVTP201 0-0-1	PC8: Digital IC Design 23EVTC209 2-0-1	PCLx: CMOS VLSI Circuits Lab 24EVTP301 0-0-1	H3: Professional Aptitude and Logical reasoning. 16EHSC301 3-0-0	P3: Senior Design Project 25EVTW401 0-0-6	
			PCL2: Analog Electroni Circuits Lab 23EVTP202 0-0-1	PCL3: LIC Lab 23EVTP203 0-0-1	P1: Mini Project 24EVTW301 0-0-3	ES4: Industry Readines & Leadership Skills 23EHSA304 0-0-0	CIPE & EVS 15EHSC402 Audit	
			ES2: Microcontroller Architecture & Programming 23EVTF201 2-0-1 C Programming (Dip) 23EVTF202 0-0-2	PCL3: Data Structure Applications Lab 23EVTF203 0-0-2 PCL3: Data Structure Lab (Diploma) 23EVTF204 0-0-3	ES3: Arithmetical Thinking & Analytica Reasoning 23EHSA303 0-0-0			
Credits	**22**	**22**	**25.5**	**24.5**	**25**	**23**	**21**	**17**

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Curriculum Structure-Semester wise

Semester - I

No	Code	Course	Category	L-T-P	Credits	Contact Hours	ISA	ESA	Total	Exam Duration (in hrs)
1	18EMAB101	Single Variable Calculus	BS	4-1-0	5	6	50	50	100	3 hrs
2	15ECHB102	Engineering Chemistry	BS	3-0-0	3	3	50	50	100	3 hrs
3	15ECVF101	Engineering Mechanics	ES	4-0-0	4	4	50	50	100	3 hrs
4	18ECSP101	C Programming for Problem solving	ES	0-0-3	3	6	80	20	100	3 hrs
5	18EEEF101	Basic Electrical Engineering	ES	3-0-0	3	3	50	50	100	3 hrs
6	20EHSP101	Design Thinking for Social Innovation	HSS	0-1-1	2	3	50	50	100	1.5hrs
7	15EHSH101	Professional Communication	HSS	1-1-0	2	3	50	50	100	1.5 hrs
TOTAL				**15-3-4**	**22**	**27**	410	290	700	

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Semester - II

No	Code	Course	Category	L-T-P	Credits	Contact Hours	ISA	ESA	Total	Exam Duration (in hrs)
1	18EMAB102	Multivariable Calculus	BS	4-1-0	5	6	50	50	100	3 hrs
2	15EPHB101	Engineering Physics	BS	3-0-0	3	3	50	50	100	3 hrs
3	18ECSP102	Problem Solving with Data Structures	ES	0-0-3	3	6	80	20	100	3 hrs
4	15ECRP101	Engineering Exploration	ES	0-0-3	3	6	80	20	100	3 hrs
5	18EECF101	Basic Electronics	ES	4-0-0	4	4	50	50	100	3 hrs
6	15EMEF101	Basic Mechanical Engineering	ES	2-1-0	3	4	50	50	100	3 hrs
7	16EPHP101	Applied Physics Lab	BS	0-0-1	1	2	80	20	100	3 hrs
TOTAL				**13-2-7**	**22**	**32**	**410**	**290**	**700**	

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Semester- III

No	Code	Course	Category	L-T-P	Credits	Contact Hours	ISA	ESA	Total	Exam Duration (in hrs)
1	15EMAB203	BS: Integral Transforms and Statistics	BS	4-0-0	4	4	50	50	100	3 hours
2	22EHSH201	ES1: Corporate Communication	ES	0.5-0-0	0.5	1	100	--	100	3 hours
3	23EVTC201	PC1: Circuit Analysis	PC	4-0-0	4	4	50	50	100	3 hours
4	23EVTC202	PC2: Analog Electronic Circuits	PC	4-0-0	4	4	50	50	100	3 hours
5	23EVTC203	PC3: Digital Circuits	PC	4-0-0	4	4	50	50	100	3 hours
6	23EVTC204	PC4: Signals & Systems	ES	4-0-0	4	4	50	50	100	2 hours
7	23EVTP201	PCL1: Digital Circuits Lab	PC	0-0-1	1	2	80	20	100	2 hours
8	23EVTP202	PCL2: Analog Electronic Circuits Lab	PC	0-0-1	1	2	80	20	100	2 hours
9	23EVTF201 23EVTF202	ES2: Microcontroller Architecture & Programming C Programming (Dip)	ES	2-0-1 0-0-2	3 2	4 4	80	20	100	2 hours
TOTAL				**22.5-0-3**	**25.5**	**29**	**590**	**310**	**900**	

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Semester- IV

No	Code	Course	Category	L-T-P	Credits	Contact Hours	ISA	ESA	Total	Exam Duration (in hrs)
1	15EMAB208	BS: Linear Algebra &Partial Differential Equations	BS	4-0-0	4	4	50	50	100	3 hours
2	23EHSH202	ES2: Problem Solving & Analysis	ES	0.5-0-0	0.5	1	100	--	100	3 hours
3	23EVTC205	ES4: Semiconductor Device Physics	PC	3-0-0	3	3	50	50	100	3 hours
4	23EVTC206	PC5: Linear Integrated Circuits	PC	4-0-0	4	4	50	50	100	3 hours
5	23EVTC207	PC6: Computer Architecture	PC	2-0-1	3	4	50	50	100	3 hours
6	23EVTC210	PC7: ARM Processor & Applications	PC	3-0-1	4	5	50	50	100	3 hours
7	23EVTC209	PC8: Digital IC Design	PC	2-0-1	3	4	80	20	100	2 hours
8	23EVTP203	PCL3: LIC Lab	PC	0-0-1	1	2	80	20	100	2 hours
9	23EVTF203	PCL3: Data Structure Applications Lab	ES	0-0-2	2	4	80	20	100	2 hours
10	23EVTF204	PCL3: Data Structure Lab (Diploma)		0-0-3	3	6				
TOTAL				**18.5-0-6**	**24.5**	**31**	**590**	**310**	**900**	

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Semester- V

No	Code	Course	Category	L-T-P	Credits	Contact Hours	ISA	ESA	Total	Exam Duration (in hrs)
1	24EVTC301	PC10: CMOS VLSI Design	PC	4-0-0	4	4	50	50	100	3 hours
2	24EVTC302	PC11: Control Systems	PC	4-0-0	4	4	50	50	100	3 hours
3	24EVTC303	PC12: Machine Learning & Deep Learning	PC	2-0-2	4	6	50	50	100	3 hours
4	24EVTC304	PC13: Electromagnetic Fields and Waves	PC	3-0-0	3	3	50	50	100	3 hours
5	24EVTC305	Digital Signal Processing and Architecture	PC	3-0-0	3	4	50	50	100	2 hours
6	24EVTC306	Analog Integrated Circuit Design	PC	2-0-1	3	4	50	50	100	3 hours
7	24EVTP301	PCLx: CMOS VLSI Design Lab	PC	0-0-1	1	2	80	20	100	2 hours
8	24EVTW301	P1: Mini Project	PW	0-0-3	3	6	50	50	100	2 hours
9	23EHSA303	ES3: Arithmetical Thinking & Analytical Reasoning	Audit	0-0-0	Audit	1	100	--	100	3 hours
TOTAL				**18-0-7**	**25**	**34**	**580**	**320**	**900**	

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Semester- VI

No	Code	Course	Category	L-T-P	Credits	Contact Hours	ISA	ESA	Total	Exam Duration (in hrs)
1	24EVTC307	Physical Design-Analog	HC	1-0-2	3	4	67	33	100	2 hours
2	24EVTC308	PC14: VLSI Fabrication Technology	PC	2-0-0	2	2	50	50	100	2 hours
3	24EVTC309	System Verilog for Verification	PC	1-0-2	3	4	67	33	100	2 hours
4	24EVTC310	GEN AI	PC	2-0-1	3	4	67	33	100	2 hours
5	24EVTExxx	PSE Elective 1	PE	3-0-0	3	3	50	50	100	3 hours
6	24EVTW302	P2: Minor Project	PW	0-0-6	6	12	50	50	100	2 hours
7	16EHSC301	H3: Professional Aptitude and Logical reasoning	HC	3-0-0	3	3	50	50	100	3 hours
8	23EHSA304	ES4: Industry Readiness & Leadership Skills	ES	0-0-0	Audit	1	25	75	100	3 hours
TOTAL				**12-0-11**	**23**	**33**	**426**	**374**	**800**	

Semester- VII

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No	Code	Course	Category	L-T-P	Credits	Contact Hours	ISA	ESA	Total	Exam Duration (in hrs)
1	25EVTC401	PC16: CMOS ASIC Design	PSC	1-0-2	3	3	67	33	100	2 hours
2	25EVTExxx	PSE Elective 2	PSE	3-0-0	3	3	50	50	100	3 hours
3	25EVTExxx	PSE Elective 3	PSE	3-0-0	3	3	50	50	100	3 hours
4	25EVTExxx	PSE Elective 4	PSE	3-0-0	3	3	50	50	100	3 hours
5	25EVTExxx	PSE Elective 5	PSE	3-0-0	3	3	50	50	100	3 hours
6	25EVTW401	P3: Senior Design Project	PW	0-0-6	6	12	50	50	100	3 hours
7	15EHSC402	CIPE & EVS	M	2-0-0		2	50	50	100	3 hours
TOTAL				**15-0-6**	**21**	**29**	**350**	**350**	**700**	

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Semester- VIII

No	Code	Course	Category	L-T-P	Credits	Contact Hours	ISA	ESA	Total	Exam Duration (in hrs)
1	24EVTE	PSE Elective 6	PSE	3-0-0	3	3	50	50	100	3 hours
2	24EVTO	Open Elective 1	OE	3-0-0	3	3	50	50	100	3 hours
OR										
3	24EVTI493	Internship- Training	PRJ	0-0-6	6	12	50	50	100	3 hours
And										
	24EVTW494	Internship- Project	PRJ	0-0-11	11	22	50	50	100	3 hours
OR										
4	24EVTW402	Project Work	PRJ	0-0-11	11	22	50	50	100	3 hours
TOTAL				**6-0-11**	**17**	**28**	**150**	**150**	**300**	

Semester	**I**	**II**	**III**	**IV**	**V**	**VI**	**VII**	**VIII**	**Total**

Credits	**22**	**22**	**25.5**	**24.5**	**25**	**23**	**21**	**17**	**180**

List of Program Electives VI Sem

Sr.No	Name of the Course	Course Code
1.	Communication Systems	24EVTE301
2.	Computer Communication Networks	24EVTE302
3.	Embedded Intelligent Systems	24EVTE303
4.	Advanced IC packaging	24EVTE304
5.	Automotive Electronics	24EVTE305

List of Program Electives VII & VIII Sem

Sr.No	Name of the Course	Course Code
1.	Memory Design and Testing	25EVTE401
2.	Design For Testability	25EVTE402
3.	System on Chip (SoC) Design	25EVTE404
4.	Design and Analysis of Algorithm	25EVTE405
5.	RF Circuit Design	25EVTE406
6.	Hardware-Software Co-design	25EVTE407
7.	Computer-Aided VLSI Design	25EVTE408
8.	Power Management IC (Swayam)	25EVTE409
9.	Testing & Characterization	25EVTE410
10.	Phase Locked Loop(Swayam)	25EVTE411
11.	Advanced Computer Architecture	25EVTE412
12.	Analog and Mixed mode VLSI Circuits	25EVTE413
13.	OOPS using C++	25EVTE414
14.	MEMS	25EVTE415
15.	EMC & Signal Integrity	25EVTE416
16.	Low Power VLSI Circuits	25EVTE417
17.	VLSI Interconnects	25EVTE418
18.	Advanced DFT for ASIC Design	25EVTE419

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List of Open Electives VIII Sem

Sr.No	Name of the Course	Course Code
1	Hardware-Software Co-design	24EVTO401
2	System on Chip (SoC) Design	24EVTO402

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Curriculum Content- Course wise

Program: Electronics Engineering (VLSI Design & Technology)		Semester: I
Course Title: Single Variable Calculus		Course Code: 18EMAB101
L-T-P: 4-1-0	Credits: 5	Contact Hours:5 hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 50Hrs	Examination Duration: 3 Hrs	

Unit I

1. Functions, Graphs and Models

Functions, types of functions, transformations and models (Linear, exponential, trigonometric).
MATLAB: Graphing functions, Domain-Range and Interpreting the models

2. Calculus of functions and models

Limit of a function, Infinite limits- graph, Continuity and discontinuity, Intermediate value theorem statement, Roots of the equation using Bisection Method and Newton- Raphson Method
Interpretation of derivative as a rate of change, All the rules of derivatives (List only), Maxima, Minima and optimization problems. Curvature and Radius of Curvature, Indeterminate forms, L-Hospital's rule-Examples
MATLAB: optimization problems. Curvature problems

Unit II

3. Infinite Series

Definition, Convergence of series, Tests of convergence – p-series, Alternating series. Power series, radius of convergence, Taylor's and Maclaurin's series, Applications of Taylor's and Maclaurin's series
MATLAB: Convergence of series

4. Integral calculus

Tracing of standard curves in Cartesian form, Parametric form and Polar form; Beta and gamma function, relation between them, evaluation of integrals using Beta and gamma functions; Applications to find arc length, Area, Volume and surface area (Cartesian, parametric and polar curves). Approximate integration- Trapezoidal rule, Simpson's 1/3 rule
MATLAB: problems on arc length, area, volume and surface area

Unit III

5. Ordinary differential equations of first order

(a) Introduction to Initial Value problems. Linear and Bernoulli's equations, Exact equations and reducible to exact form, Numerical solution to Initial Value problems-Euler's method, Modified Euler's method and Runge-Kutta method
(b) Applications of first order differential equations-Orthogonal trajectories growth and decay problems, mixture problems, Electrical circuits, falling bodies.
MATLAB: Solve differential equations

Text Books

1. Early Transcendentals Calculus- James Stewart, Thomson Books, 7ed 2010.

Reference Books:

1. Calculus Single and Multivariable, Hughues-Hallett Gleason, Wiley India Ed, 4ed, 2009.

2. Thomas Calculus, George B Thomas, Pearson India, 12ed, 2010

Back to Semester - I

Program: Electronics Engineering (VLSI Design & Technology)		Semester: I
Course Title: Engineering Physics		Course Code: 15EPHB101
L-T-P: 3-0-0	Credits: 3	Contact Hours:3 hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 50Hrs	Examination Duration: 3 Hrs	

Unit I

Chapter 1: Conduction in semiconductors

Atomic theory: The atom, electron orbits and energy levels, energy bands, Conduction in solids: Electron motion and hole transfer, conventional current and electron flow

Conductors, semiconductors and insulators: Bonding force between atoms, Energy bands in different materials.

n-type and p-type Semiconductors: Doping, n-Type material, p-Type material, Majority and minority charge carriers, Effects of heat and light, charge carrier density.

Semiconductor conductivity: Drift current, diffusion current, charge carrier velocity, conductivity, Hall Effect.

(Text 1 Page No 1-33)

Chapter 2: Junctions

The pn-Junctions: Junction of p-Type and n-Type, Barrier voltage, depletion region, Qualitative theory of p-n Junction

Biased junctions: Reverse biased junction, forward biased junction, junction temperature effects.

Junction currents and voltages: Shockley equation, junction currents, junction voltages.

p-n Junction Diode characteristics and parameters: Forward and reverse characteristics, diode parameters.

Diode approximations: Ideal diode and practical diodes, piecewise linear characteristics, DC equivalent circuits.

DC load line analysis: DC load line, Q-Point, calculating load resistance and supply voltage.

Temperature Effects: Diode power dissipation, forward voltage drop, dynamic resistance.

Diode AC models: Junction capacitance, AC-equivalent circuits (Reverse biased and forward biased), reverse recovery time.

Diode specifications: Diode data sheets, low power diodes, rectifier diodes

Diode testing: Ohmmeter tests, use of digital meter, plotting diode characteristics.

Zener diodes: Junction break down, circuit symbols and packages, characteristics and parameters, data sheet, equivalent circuits.

(Text 1 Page No 34-71)

Unit II

Chapter 3: Electrostatics

Review on vectors:

Coordinate Systems, Vector and Scalar Quantities, Properties of Vectors, Components of a Vector and Unit Vectors

(Text 2 Page No 59-77)

Electric Fields:

Properties of Electric Charges, Charging Objects by Induction, Coulomb's Law, Analysis Model: Particle in a Field (Electric), Electric Field of a Continuous Charge Distribution, Electric Field Lines Motion of a Charged Particle in a Uniform Electric Field

Gauss's Law:

Electric Flux, Gauss's Law, Application of Gauss's Law to Various Charge Distributions, Conductors in Electrostatic Equilibrium
Electric Potential:
Electric Potential and Potential Difference, Potential Difference in a Uniform Electric Field, Electric Potential and Potential Energy Due to Point Charges, Obtaining the Value of the Electric Field from the Electric Potential, Electric Potential Due to Continuous Charge Distributions Electric Potential Due to a Charged Conductor, Applications of Electrostatics
Capacitance and Dielectrics:
Definition of Capacitance, Calculating Capacitance, Combinations of Capacitors, Energy Stored in a Charged Capacitor, Capacitors with Dielectrics, Electric Dipole in an Electric Field, An Atomic Description of Dielectrics
(Text 2 Page No 690-807)

Unit III
Chapter 4: Electromagnetics
Magnetic Fields:
Analysis Model: Particle in a Field (Magnetic), Motion of a Charged Particle in a Uniform Magnetic Field, Applications Involving Charged Particles Moving in a Magnetic Field, Magnetic Force Acting on a Current-Carrying Conductor, Torque on a Current Loop in a Uniform Magnetic Field,
Sources of the Magnetic Field:
The Biot–Savart Law, The Magnetic Force Between Two Parallel Conductors, Ampere's Law, The Magnetic Field of a Solenoid, Gauss's Law in Magnetism, Magnetism in Matter
Faraday's Law:
Faraday's Law of Induction, Motional emf, Lenz's Law, Induced emf and Electric Fields Generators and Motors, Eddy Currents
(Text 2 Page No 868-969)

Text Book:

1. David A Bell, "Electronics Devices and Circuits", Fifth Edition, Oxford University Press.
2. Serway and Jewett, "Physics for Scientists and Engineers-with Modern Physics", 9th Edition, CENGAGE learning. 2014

Reference Books:

1. Jacob Millman and Christos Halkias, "Electronic Devices and Circuits" TMH
2. R P Feynman, Robert B Leighton , Matthew Sands, The Feynman Lectures on Physics Vol-II, Norosa Publishing House (1998).
3. Ben G Streetman, Solid State Electronic Devices, Prentice Hall, 1995

Back to Semester - I

Program: Electronics Engineering (VLSI Design & Technology)		Semester: I
Course Title: Engineering Mechanics		Course Code: 15ECVF101
L-T-P: 4-0-0	Credits: 4	Contact Hours:4 hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 50Hrs	Examination Duration: 3 Hrs	

Unit I

Chapter 1: Overview of Civil Engineering

Evolution of Civil Engineering
Specialization, scope and role.
Impact of Civil Engineering on
National economy, environment and social & cultural fabric.
Challenges and Opportunities for Civil Engineers
Civil Engineering Marvels, Future challenges, Higher education and Research.

Chapter 2: Coplanar concurrent force system

Introduction to Engineering Mechanics:
Basic idealizations – Particle, Continuum, Body, Rigid body, Deformable body, Definition of force and its elements; Laws of Mechanics – Parallelogram law of forces, Principle of transmissibility, Law of Superposition, Newton's laws of motion. Classification of force systems
Resultant of coplanar concurrent force system: Definitions – Resultant, composition & Resolution of a force, Equilibrium, Equilibrant, Formulae for resultant of forces and resolution of a force. Numerical problems on resultant of forces.
Equilibrium of coplanar concurrent force system:
Conditions of equilibrium, Action & Reaction, Free body diagram, Lamis' theorem. Numerical problems on equilibrium of forces.

Chapter3:Coplanar non-concurrent force system

Resultant of a force system: Moment, moment of a force, couple, moment of a couple, Characteristics of couple, Equivalent force-couple system, Numerical problems on moment of forces and couples, on equivalent force-couple system. Varignons principle of moments, Resultant of coplanar- non-concurrent force systems and numerical problems.

Unit II

Chapter4:Equilibrium of a force system (Chapter 3 contd..)

Conditions of equilibrium, types of support and loading for a statically determinate beam, Reactions at support connections, Numerical problems on equilibrium of force systems and support reactions for a statically determinate beam.

Chapter 5: Static Friction

Introduction, types of friction, definition, limiting friction, coefficient of friction, laws of Coulomb friction, angle of friction and angle of repose, cone of friction. Wedge and belt friction theory. Derivation of belt friction formula. Numerical problems on, impending motion on horizontal and inclined planes (including connected bodies); wedge friction; Ladder friction and Belt friction.

Chapter 6: Simple Stress and Strain

Introduction, Properties of Materials, Stress, Strain, Elasticity, Elastic limit, Hooke's law & Young's modulus, Stress – Strain Diagram for structural steel, working stress and Factor of safety. Deformation of a bar due to force acting on it. Law of super position. Stresses in bars of uniform & varying cross sections. Composite sections. Problems connected to above topics.

Unit III

Chapter 7: Centroid of Plane Figures

Introduction, Definition, Methods of determining the centroid, axis of reference, axis of symmetry, Locating the centroid of simple plane figures (triangle, semicircle, quarter of a circle and sector of a circle etc,.) using method of integration, Numerical problems on Centroid of simple built up sections.

Chapter 8: Second moment of area (Plane figures)

Introduction, Definition, Method of determining the second moment of area, Section Modulus, Radius of gyration, perpendicular and Parallel axis theorems, Polar second moment of area, second moment of area of simple plane figures (triangle, rectangle, semicircle, circle etc,.) using method of integration, Numerical problems on MI of simple built up sections.

Text Books

1. Beer, F.P. and Johnston, R., *Mechanics for Engineers: Statics*, McGraw Hill Company, New York, 1988.
2. Bhavikatti, S.S., and Rajasshekarappa K.G., *Engineering Mechanics*, 3Ed., New Age International Pub. Pvt. Ltd., New Delhi, 2008.
3. Kumar, K.L., *Engineering Mechanics*, 3ed., Tata McGraw Hill Publishing Company, New Delhi, 2003.
4. Punmia, B.C., Jain, A. and Jain, A., *Mechanics of Materials*, Lakshmi Publications, New Delhi, 2006

Reference Books:

1. Jagadeesh, T.R. and Jayaram, *Elements of Civil Engineering*, Sapna Book House, Bangalore, 2006.
2. Ramamrutham, S., *Engineering Mechanics*, Dhanpat Rai Publishing Co., New Delhi, 1998.
3. Singer, F.L., *Engineering Mechanics*, 3rd edition Harper Collins, 1994.
4. Timoshenko, S.P. and Young, D.H., *Engineering Mechanics*, 4th edition, McGraw Hill Publishing Company, New Delhi, 1956.
5. Irving H Shames, *Engineering Mechanics*, 3rd edition, Prentice-Hall of India Pvt. Ltd, New Delhi- 110 001, 1995.

Back to Semester - I

Program: Electronics Engineering (VLSI Design & Technology)		Semester: I
Course Title: C Programming for Problem solving		Course Code: 18ECSP101
L-T-P: 0-0-3	Credits: 3	Contact Hours:6 hrs/week
ISA Marks: 80	ESA Marks: 20	Total Marks: 100
Teaching Hours: 78Hrs	Examination Duration: 3 Hrs	

Introduction to Problem solving

Introduction to algorithms / flowcharts and its notations, top down design, elementary problems.

Basics of C programming language

Characteristics and uses of C, Structure of C program, C Tokens: Keywords, Identifiers, Variables, Constants, Operators, Data-types, Input and Output statements.

Decision control statements

Conditional branching statements: if statement, if else statement, else if ladder, switch statement, unconditional branching statements: break, continue.

Introduction to Debugging Skills

Introduction to Test Driven Programming.

Iterative statements

while, do while, for, nested statements

Functions

Introduction, Function declaration, definition, call, returns statement, passing parameters to functions, introduction to macros.

Introduction to Coding Standards

Arrays and Strings

Introduction, Declaration, Accessing elements, Storing values in arrays, Operations on one dimensional array, Operations on two dimensional arrays,

Introduction to Code Optimization and refactoring

Pointers

Introduction, declaring pointer, pointer variables, pointer expression and arithmetic, passing arguments to functions using pointers, pointers and arrays, passing an array to a function.

Structures and Unions

Introduction, passing structures to functions, Array of structures, Unions

Text Books

1. R.G.Dromey, How to Solve it by Computer, 1ed, PHI, 2008.
2. Yashvant Kanetkar, Let us C ,15th ed, BPS Publication, 2016.

Reference Books:

1. B W Kernighan, D M Ritchie, The Programming language C, 2ed, PHI, 2004.
2. B S Gottfried, Programming with C, 2ed, TMH, 2006.
3. B.A. Forouzan, R.F. Gilberg, A Structured Program Approach Using C, 3ed, CENGAGE Learning, 2008.

Program: Electronics Engineering (VLSI Design & Technology)		Semester: I
Course Title: Basic Electrical Engineering		Course Code: 18EEEF101
L-T-P: 3-0-0	Credits: 3	Contact Hours:3 hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 40Hrs	Examination Duration: 3 Hrs	

Unit I

Overview of Electrical Engineering

Specialization, scope & role, impact of Electrical Engineering on national economy, environment, Sources of generation, sustainability, challenges and opportunities for electrical engineers, electrical engineering marvels, future challenges.

DC Circuits

Voltage and current sources, Kirchoff's current and voltage laws, loop and nodal analysis of simple circuits with dc excitation. Time-domain analysis of first-order RL and RC circuits.

AC Circuits

Representation of sinusoidal waveforms, peak and rms values, phasor representation, real power, reactive power, apparent power, power factor. Analysis of single-phase series and parallel R-L-C ac circuits. Three-phase balanced circuits, voltage and current relations in star and delta connections. power measurement using two watt meters

Unit II

Electrical Actuators

Electromagnetic principles, Solenoid, Relays, classification of Electric motors, DC motors-shunt, series, compound, separately excited, PMDC motors – Speed Control, Stepper Motors, BLDC motors, three phase induction motor, Characteristics and applications, selection of motors for various applications.

Power Electronics (Text1, chapter 45)

Introductory, Thyristor, Some thyristor circuits, Limitations to thyristor operation, The thyristor in practice, The fully controlled AC/DC converter, AC/DC inversion, Switching devices in inverters, Three-phase rectifier networks, The three-phase fully controlled converter, Inverter-fed induction motors, Soft-starting induction motors, DC to DC conversion switched-mode power

Unit III

Electrical Wiring, Safety and protection(Ref :Text3-page 1 to 10)

Types of wires and cables for internal wiring, Types of switches and Circuits, Types of wiring, Safety precautions and rules in handling electrical appliances, Electric shock, first aid for electrical shocks, Importance of grounding and earthing, Methods for earthing, Fuses, MCB, ELCB and Relays, Lockout and Tagout, Electrical Codes and Standards.

Batteries:

Basics of lead acid batteries, Lithium Ion Battery , Battery storage capacity, Coulomb efficiency, Numerical of high and low charging rates, Battery sizing. Numericals.

Text Books

1. Hughes, Electrical & Electronic Technology, 8th , Pearson Education, 2001
2. P C Sen, Principals of Electrical Machines and Power Electronics, 2nd, Wiley Publications
3. Gilbert M Masters, Renewable and efficient Electrical Power systems, Published by John Wiley & Sons 2004 edition
4. Frank D. Petruzella, Electric Motors and Control Systems, McGraw Hill Education Private Limited 2009 Edition

Reference Books:

1. D C Kulshreshtha, Basic Electrical Engineering, Mc Graw Hill Publications
2. David G Alciatore and Michel B Histand, Introduction to Mechatronics and Measurement Systems, 3rd, Tata McGraw Hill Education Private Limited, New Delhi., 2005
3. Vincent Del Toro, Electrical Engineering Fundamentals, 2nd edition Prentice Hall India

Back to Semester - I

Program: Electronics Engineering (VLSI Design & Technology)		**Semester: I**
Course Title: Design Thinking for Social Innovation		**Course Code: 20EHSP101**
L-T-P: 0-1-1	**Credits: 2**	**Contact Hours:3 hrs/week**
ISA Marks: 80	**ESA Marks: 20**	**Total Marks: 100**
Teaching Hours: 28Hrs	**Examination Duration: 3 Hrs**	

Module		Topics	Assignments	Support activities / Tools
KNOWLEDGE, TOOLS & DEVELOPMENT	Course sensitization	1. Introduction to Social Innovation: • Awakening social consciousness **(www.yourstory.com)** • Social Innovation and Leadership • Engineering& Social innovation (EPICS) **(Connecting SI Course to Mini Project, Capstone Project, Campus Placements)** • Course Overview • **Students' Self Introduction Activity** • Group formation **Activity**	**Reading assignments** • Read the handout on "The Process of Social Innovation" by Geoff Mulgan • Design thinking for Social Innovation **Written Assignments** • **Writing about Akshaya Patra in class.** **(Background information about Akshaya patra and the Social Cuase it is addressing)** • **Brainstorming Session on Social Innovators in Class**	• Class activity on Behavioral Blocks to Innovation **Discussion on the behavioural blocks.** • **Introducing oneself with three Adjectives- Appreciating diversity and discovering self** • **Group Formation Activity (Forming square)** **(Making four equilateral triangles out of popsicle sticks to enhance group cohesiveness amongst the group mates)**
	Create Mindsets	**Seven Mindsets:** 1. Empathy **(Example of The Boy and the Puppies)** 2. Optimism **(Person Paralyzed waist down / Glass Halh full Half Empty)** 3. Iteration **(Thomas Alva Edison)** 4. Creative Confidence **(Origamy – Josef Albers)** 5. Making it 6. Embracing Ambiguity **(Confusion is the Welcome doormat at the door of Creativity)** 7. Learning from Failure	**Reading assignments** • Handout on " Create Mindsets"	• **(How to train the Dragon? Common Video for all the mindsets)** • **Watching in Class TED Talk on "How to build youir Creative Confidence by David Kelley – IDEO Founder)**

		(Designing Website first and then asking the stakeholders about the website) **(Spending one lakh for the business which is never launched)**		
	Process of Social Innovation	**Engage** Community study and Issue Identification	**Reading assignments** • Handout on Community Study and Issue Identification • Case Study on "EGramSeva" • Case Study on "Janani Agri Serve" **Class Presentations** • Initial observations being made by the group **(Literature Survey of Places of Hubli-Dharwad)** **www.readwhere.com** • Detailed interaction / engagements with the society and finalize the social issue for intervention **Use template 1: Frame your Design Challenge**	• Activity on Observation skills To know how to use one's observation skills in understanding the social conditions • Experience sharing by senior students • Brainstorming Deliberations on the initial observations and arrive at the "Social Issue" • Familiarization of the respective templates with the help of sample case study
		PEER REVIEW		
		2. Inspiration • Plan for the Research • Development of Interview guide • Capture your Learnings	**Reading assignments** • Handout on Overview of Inspiration **Class Presentations** • Entirety of the Social Issue • Identification of the Stake Holders	• Familiarization of the respective templates with the help of sample case study

			(Examples on Fluoroscent Curtain and Students' Punctuality for Class) • Interview Questions **(Role Play on Interview with Stakeholders)** • Category wise Learnings capture **Use template 2: Plan your Research** **Template 3. Development of Interview Guide** **Template 4. Capture your Learning**	
		3. Ideation **3.1 Synthesis** • Search for meaning • Create "How might we" question	**Reading assignments** • Handout on Overview of Ideation-Synthesis **Class Presentations** • Create insights • "How might we" questions **Use template 5: Create Insights** **Template 6: Create "How Might We' Questions**	• Familiarization of the respective templates with the help of sample case study
		3.0 Ideation **3.2 Prototyping** • Generate Ideas • Select Promising Ideas • Determine what to prototype • Make your prototype	**Reading assignments** • Handout on Overview of Ideation-Prototyping **Class Presentations** • Story board-demonstrating the possible solutions **Use template 7: Select your best ideas**	• Brain storming • Familiarization of the respective templates with the help of sample case study • Activity on Risk management • Activity on Resource management

		• Test and get feedback	**Template 8 : Determine what to prototype**	Structure building games
		PEER REVIEW		
		4.0 Implementation • Create an action plan • Community Partners (if any) • Budgeting & Fundraising 1. Peer to Peer 2. Crowd Funding 3. Giving Kiosks 4. Donation 5. Envelop Funding 6. Marathons/ Walkathons 7. Conducting Yoga Classes (www.causevox.com / www.blog.fundly.com) • Duration • Ethical concerns • Launch your solution • Feedback (Impact)	**Reading assignments** • Handout on Overview of Implementation **Class Presentations** • Pilot implementation plan with required resources and Budget indicating stake holders & their enagement	• Familiarization of the respective templates with the help of sample case study
		5.0 Reflect Reflection of the overall learning by the students	**Reading assignments** • Handout on Overview of students Reflection **Use template 9: Reflection on the Process** **Class Presentations**	• Familiarization of the respective templates with the help of sample case study

			Final Presentation- After Implementation		

Back to Semester - I

Program: Electronics Engineering (VLSI Design & Technology)		Semester: I
Course Title: Applied Physics lab		Course Code: 16EPHP101
L-T-P: 0-0-1	Credits: 1	Contact Hours:2 hrs/week
ISA Marks: 80	ESA Marks: 20	Total Marks: 100
Teaching Hours: 24Hrs	Examination Duration: 3 Hrs	
List of Experiments		
1. Four probe method		
2. V-I characteristics of p-n junction diode		
3. Zener diode characteristics		
4. Hysteresis loss		
5. Transistor characteristics		
6. Measurement of dielectric constant		
7. Resonance frequency of LCR circuits		
8. Study of frequency response of passive components		
9. Calibration of thermocouple		
10. Calibration of electrical meters		

Back to Semester - I

Program: Electronics Engineering (VLSI Design & Technology)		Semester: II
Course Title: Multivariable calculus		Course Code: 18EMAB102
L-T-P: 4-1-0	Credits: 5	Contact Hours:5 hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 50Hrs	Examination Duration: 3 Hrs	

Unit I

1. **Partial differentiation**
   Function of several variables, Partial derivatives, Level curves, Chain rule, Errors and Approximations. Extreme value problems. Lagrange's multipliers.
2. **Double integrals**
   Double integrals- Rectangular and polar coordinates, Change the order of integration. Change of variables, Jacobian. Application of double integrals

MATLAB: optimization problems, application of double integrals

Unit II

3. **Triple integrals**

   Triple integrals, Cartesian, change to Cylindrical and Spherical coordinates Application of Triple integrals

4. **Calculus of Vector Fields**

   Vector fields, Gradient and directional derivatives. Line and Surface integrals. Independence of path and potential functions. Green's theorem, Divergence of vector field, Divergence theorem, Curl of vector field. Stokes theorem.

MATLAB: application of Triple integrals, Vector calculus problems

Unit III

5. **Differential equations of higher orders**
   (a) Linear differential equations of second and higher order with constant coeffiISAntsThe method of Variation of parameters. Initial and boundary value problems.
   (b) Applications of second order differential equations-Newton's 2nd law, electrical circuits, Simple Harmonic motion. Series solution of differential equations. Validity of Series solution of Differential equations.

MATLAB: application of differential equations

Text Books

1. Early Transcendentals Calculus- James Stewart, Thomson Books, 7ed 2010.

Reference Books:

1. Calculus Single and Multivariable, Hughues-Hallett Gleason, Wiley India Ed, 4ed, 2009.
2. Thomas Calculus, George B Thomas, Pearson India, 12ed, 2010

Back to Semester - II

Program: Electronics Engineering (VLSI Design & Technology)		Semester: II
Course Title: Engineering Chemistry		Course Code: 15ECHB102
L-T-P: 3-0-0	Credits: 3	Contact Hours:3 hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 50Hrs	Examination Duration: 3 Hrs	

Unit I

1. Chemical Bonding

Introduction, Ionic bond, factors influencing the formation of Ionic bond: Ionization energy. Electron affinity & electro negativity and properties of Ionic compounds. Covalent bond: Valence Bond theory & Molecular Orbital theory – formation of hydrogen molecule, factors influencing the formation of covalent bond, polar and non-polar covalent bond, dipole moment, problems on calculation of percentage of Ionic character and properties of covalent compounds, Co-ordinate bond: formation of hydronium ion and ammonium ion.

2. Electrochemical Energy Systems

Electrode potential, Nernst equation, formation of a cell; Reference electrodes – Calomel electrode, Determination of electrode potential, numerical problems on E, E_{cell} & E^0_{cell}.

Batteries: Classification, Characteristics, Lead - acid, Lithium ion battery. Fuel cells - Methonol-O_2 fuel cell.

3. Polymers

Introduction, polymerization ; mechanism of polymerization taking ethylene as an example. Determination of molecular weight of a polymer – numerical problems. Commercial polymers - Plexi glass, PS, polyurethane.

Polymer composites: Carbon fiber and Epoxy resin – synthesis, properties and applications. Introduction to conducting polymers, mechanism of conduction in poly acetylene and applications.

Unit II

4. Plating Techniques

Introduction, technological importance. Electroplating, Principles of electroplating. Factors affecting nature of electrodeposit, throwing power, Numerical problems on throwing power, Electroplating process of gold by acid cyanide bath. Electro less plating, advantages of electro less plating over electroplating. Electro less plating of Cu and its application in the manufacture of PCB.

5. Wafer Technology

Introduction, physical and chemical properties of silicon. Purification of silicon; chemical vapor deposition (CVD) process, zone refining process. Crystal growth; preparation of single crystal silicon by Czhochralski crystal pulling technique – numerical problems. Crystal slicing and wafer preparation. Fabrication process: thermal oxidation, diffusion, ion implantation – numerical problems, epitaxial growth, masking and photolithography, wet etching, dry etching.

6. Material Chemistry

Liquid Crystals – Types of liquid crystals, applications of Liquid Crystal in Display system.

Fluorescence and Phosphorescence – Jablonski diagram, Thermoelectric and Piezoelectric materials – meaning, properties and applications.

Unit III

7. Instrumental methods of measurement

Advantages over conventional methods. Electro analytical methods: Potentiometer - principle, methodology and applications. Optoanalytical methods: Colorimeter - Principle, methodology and applications.

Spectral methods of analysis : UV – Spectrophotometer - Instrumentation and applications.

8. Environmental Chemistry:

Water: Sources and ill effects of water pollutants – fluoride and nitrate; determination of total hardness of water by EDTA method – numerical problems. , Sewage: Determination of Biological Oxygen Demand by Winkler's method – numerical problems and determination of Chemical Oxygen Demand – numerical problems.

Text Books

1. A text Book of Engineering Chemistry, 1st edition, Dara. S. S, S. Chand & Co. Ltd., 2009, New Delhi.
2. A text Book of Engineering Chemistry, 16th edition, Jain P.C and Jain M, Dhanpat Rai Publications, 2006, New Delhi.

Reference Books:

1. Text book of Inorganic Chemistry, P.L.Soni, Sultan Chand, 1999, New Delhi.
2. Hand book of batteries, David Linden, Thomas B Reddy, 3rd edition Mc Graw Hill publications, 2001, New York.
3. Polymer Science, 6th Edition, Gowariker V.R., Viswanathan N.V., Sreedhar J., New Age International (P) Ltd, 2007, New Delhi.
4. Solid State Devices& Technology, 4thEdition, V.Suresh Babu, sanguine Technical Publishers, 2005, Bangalore.
5. Material Science & Engineering: An Introduction, 9th Edition, Calister William D, John Wiley and sons, 2007, New York.
6. Instrumental methods of Chemical nalysis, 5th Edition, Gurudeep R Chatwal, Shan K Anand, Himalaya Publishing House Pvt. Ltd, 2010, Mumbai.
7. VLSI Technology, 2nd Edition, S.M.Sze, McGraw Hill Series in electrical and computer engineering, 1998, New York.

Back to Semester - II

Program: Electronics Engineering (VLSI Design & Technology)		Semester: II
Course Title: Problem Solving with Data Structures		Course Code: 18ECSP102
L-T-P: 0-0-3	Credits: 3	Contact Hours:6 hrs/week
ISA Marks: 80	ESA Marks: 20	Total Marks: 100
Teaching Hours: 78Hrs	Examination Duration: 3 Hrs	

Pointers, Structures and Files

Recap of basics: Pointers ,Structures; Self-referential structures, dynamic memory management Files – File manipulation programs

Stacks and Recursion

Stack: Definition, Operations, Stack ADT Implementation of stack operations. Applications of stack.Recursion- Need for Recursion and problems on Recursion.

Queues

Queue: Definitions of Linear, Circular queues, Queue ADT Linear and circular queue operations Definition and working of Priority queue, Double ended queue; Applications of queues.

Lists

Concept of lists and dynamic memory management lists, definitions and representations: singly, doubly, circular lists. Dynamic Implementation of lists and its operations, Applications of linked lists

Binary trees

Binary Tree: Definition, Terminology and representation, Tree Traversals both recursive and iterative. Binary Search Tree and its applications.

Text Books

1. Data Structures with C -- Seymour Lipschutz, Schaum's Outline Series
2. Data Structures Using C and C++ -- Langsam and Tanenbaum, PHI Publication
3. Data Structures Through C -- Yashavant P Kanetkar, BPB Publication

Reference Books:

1. B W Kernighan, D M Ritchie, The Programming language C, 2ed, PHI, 2004.
2. B S Gottfried, Programming with C, 2ed, TMH, 2006.
3. B.A. Forouzan, R.F. Gilberg, A Structured Program Approach Using C, 3ed, CENGAGE Learning, 2008.

Back to Semester - II

Program: Electronics Engineering (VLSI Design & Technology)		Semester: II
Course Title: Engineering Exploration		Course Code: 15ECRP101
L-T-P: 0-0-3	Credits: 3	Contact Hours:6 hrs/week
ISA Marks: 80	ESA Marks: 20	Total Marks: 100
Teaching Hours: 78Hrs	Examination Duration: 3 Hrs	

List of Experiments

1. Introduction to Engineering and Engineering Study
2. Role of Analysis in Engineering, Analysis Methodology
3. Data Analysis Graphing
4. Basics of Engineering Design, Multidisciplinary Nature of Engineering Design
5. Project Management
6. Sustainability in Engineering
7. Ethics
8. Modeling, Simulation and Data Acquisition using Software Tool
9. Platform based development : Arduino
10. Course Project

Reference Books:

1. Engineering Fundamentals & Problem Solving by Arvid Eide, Roland Jenison, Larry Northup, Steven, McGraw Hill Higher Education, 6th Edition (2011)
2. Engineering Exploration (Edited Book, 2008) by Pearson Publication

Back to Semester - II

Program: Electronics Engineering (VLSI Design & Technology)		Semester: II
Course Title: Basic Electronics		Course Code: 18EECF101
L-T-P: 4-0-0	Credits: 4	Contact Hours:4 hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 50Hrs	Examination Duration: 3 Hrs	

Unit I

Chapter 1: Trends in Electronic Industries:

Introduction, Roadmap of electronic sector, scope and opportunities in various segments of electronics (i.e., Consumer, Telecom, IT, Defense, Industrial, Medical and Automobiles), Government and private sectors, Growth profile of Electronic industries, Standards and PoliISAs, Electronic System Components.

Chapter 2: Basic Components, Devices and Applications:

Diode: PN junction characteristics; modeling as a circuit element, ideal and practical diode. AC to DC converter: Half wave and full wave rectifier (centre tap and bridge), capacitor filter and its analysis, numerical examples. Zener diode and its applications (Voltage reference and voltage regulator). Realization of simple logic gates like AND and OR gates.

Chapter 3: Transistor:

BJT, transistor voltages and currents, Signal amplifier (Fixed bias, Collector base bias, Voltage divider bias, CE configuration). DC load line. Voltage, current and power gains. Transistor as a switch: NOT Gate, Basic (DTL) NAND gate. Transistor as a Small Signal Amplifier (Single Stage and Two Stage RC-coupled Amplifier).

Unit II

Chapter 4: Digital Logic:

Number systems: Decimal, Binary, Octal and Hexadecimal number systems, Conversions, Binary Operations-Addition and subtraction in binary number systems. Logic gates: Realization of simple logic functions using basic gates (AND, OR, NOT), Realization using universal gates (NAND, NOR). Boolean algebra: Theorems and postulates, DeMorgan'sTheorems , simplification of logical expressions, Karnaugh Maps, Use of Karnaugh Maps to Minimize Boolean Expressions (2 Variables, 3 Variables and 4 Variables), Design of Half Adder and Full Adder, Parallel Adder using full adders**.**

Chapter 5: Operational Amplifier:

OPAMP characteristics (ideal and practical), Linear and non-linear applications: Inverting amplifier, Non inverting amplifier, Voltage follower, Integration, Differentiation, Adder, Subtractor, ZCD and Comparator.

Unit III

Chapter 6: Communication Systems:

Basic block diagram of communication system, types of modulation. Amplitude modulation: Time-Domain description, Frequency-Domain description. Generation of AM wave: square law modulator. Detection of AM waves: envelope detector. Double side band suppressed carrier modulation (DSBSC), Generation of DSBSC wave : balanced modulator, Super heterodyne principle.

Chapter 7: Linear Power Supply, UPS & CRO:

Working principle of linear power supply, UPS and CRO. Measurement of amplitude, frequency and phase of a given signal.

Text Books

1. David A Bell, Electronic devices and Circuits, PHI New Delhi, 2004
2. K.A Krishnamurthy and M.R.Raghuveer, Electrical, Electronics and Computer Engineering for SISAntist and Engineers, 2, New Age International Publishers, 2001
3. A.P. Malvino, Electronic Principles, Tata McGraw Hill, 1999

Reference Books:

1. George Kennedy, Electronic Communication Systems, Tata McGraw Hill, 2000
2. Morris Mano, Digital logic and Computer design , 21st Indian print Prentice Hall India, 2000
3. Floyd, Digital fundamentals, 3, Prentice Hall India, 2001
4. Boylestead Nashelsky, Electronic devices & Circuit theory, Prentice Hall India, 2000
5. Ramakant Gaikawad , Operational Amplifiers & applications, PHI, 2000

Back to Semester - II

Program: Electronics Engineering (VLSI Design & Technology)		Semester: II
Course Title: Basic Mechanical Engineering		Course Code: 15EECF101
L-T-P: 2-1-0	Credits: 3	Contact Hours:4 hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 50Hrs	Examination Duration: 3 Hrs	

Unit I

Chapter 1 : Introduction to Mechanical Engineering:

Definition of engineering, Mechanical Engineering, Branches of Mechanical Engineering, Who are Mechanical Engineers?, Mechanical Engineers' top ten achievements.

Visit to Workshop and Machine Shop, Tools, Safety Precautions

Video presentations

Chapter 2: Manufacturing Engineering: Basics of Manufacturing

What is manufacturing?, The main manufacturing sectors, The importance of the main manufacturing sectors to the Indian economy, Scales of production

Classification of manufacturing Processes.

Advances in Manufacturing: CNC machines, Mechatronics and applications

Demonstration on working of Lathe, milling, drilling, grinding machines

Demonstration on Welding (Electric Arc Welding, Gas Welding, Soldering)

Demonstration and Exercises on Sheet metal work.

Visit to Learning Factory

Unit II

Chapter 3: Design Engineering: Power Transmission Elements

Overview

Design Application:

- Belt Drives. Types, Length of Belt. Velocity Ratio, Initial Tension. Ratio of Tensions. Power Transmitted, Numerical Problems.
- Gears. Spur Gear, Rack and Pinion, Worm Gear, Bevel Gear, Helical Gears. Speed, Torque, and Power in Gear pair. Simple and Compound Gear trains. Numerical Problems.
- Ball and Roller Bearings, Types, Applications.

Design Problems like a moving experience, aluminium can crusher

Video presentations

Chapter 4: Thermal Engineering 1: Prime Movers.

Internal Combustion Engines: Classification, IC engine parts, 2 stroke SI and CI engine, 4 Stroke SI and CI Engine, PV diagrams of Otto and Diesel cycles, Comparison of 2 stroke and 4 stroke

engine, comparison of CI and SI engine, Problems on Engine Performance, Future trends in IC engines.

Case study on power requirement of a bike, car or any machine
Video presentations

Unit III

Chapter 5: Thermal Engineering 2: Thermal Systems' Applications
Refrigeration system, Air conditioning system, Pumps, Blowers and Compressors, Turbines, and their working principle and specifications.

Case study on selection of various thermal systems
Video presentations

Text Books

1. Jonathan Wickert and Kemper Lewis, An Introduction to Mechanical Engineering, Third Edition, 2013- Cengage Learning.4
2. K.R.Gopalkrishna, Sudhir Gopalkrishna, S.C. Sharma. A Text Book of Elements of Mechanical Engineering, 30th Edition, Oct 2010,–Subhash Publishers, Bangalore.

Reference Books:

1. Course Material developed by the Department of Mechanical Engineering.
2. SKH Chowdhary, AKH Chowdhary, Nirjhar Roy, The Elements of Workshop Technology - Vol I & II , 11th edition 2001, Media Promoters and Publishers.
3. Basic Manufacturing, Roger Timings, Third edition, Newnes, An imprint of Elsevier

Back to Semester - II

Program: Electronics Engineering (VLSI Design & Technology)		**Semester: II**
Course Title: Professional Communication		**Course Code: 15EHSH101**
L-T-P: 1-1-0	**Credits: 2**	**Contact Hours:3 hrs/week**
ISA Marks: 50	**ESA Marks: 50**	**Total Marks: 100**
Teaching Hours: 42Hrs	**Examination Duration: 3 Hrs**	

List of Experiments

Chapter No. 1. Basics- English Communication

Course Introduction, Explanation of template mix-ups with correct usages & necessity of grammar in error detection, Usage of tenses

Chapter No. 2. Vocabulary and grammar

Vocabulary, Word Formation and Active and Passive Voice

Chapter No. 3. Bouncing Practice

Definition and types of bouncing and its practice with examples, reading skills, free style speech.Individual presentation.

Chapter No. 4. Rephrasing and Structures

Comprehension and Rephrasing, PNQ Paradigm and Structural practice.

Chapter No. 5. Dialogues

Introduction of dialogues, Situational Role plays.

Chapter No. 6. Business Communication

Covering letter, formal letters, Construction of paragraphs on any given general topic.

Reference Books:

1. Collins Cobuild Advanced Learner's English Dictionary
2. Raymond Murphy - Intermediate English Grammar, Cambridge University Press
3. Martin Hewings- Advanced English Grammar, Cambridge University Press.

Back to Semester - II

Program: Electronics Engineering (VLSI Design & Technology)		Semester: III Semester
Course Title: Integral transforms and Statistics		Course Code: 15EMAB203
L-T-P: 4-0-0	Credits: 4	Contact Hours: 4Hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 50Hrs	Examination Duration:3 Hrs	

Unit I

Chapter 1. Laplace Transforms

Definition, transforms of elementary functions- transforms of derivatives and integrals- Properties. Periodic functions, Unit step functions and Unit impulse functions.

Inverse Transforms- properties- Convolution Theorem. Initial and Final value theorems, examples; Applications to differential equations, Circuit equations.

Chapter 2: Probability

Definition of probability, conditional probability, Baye's rule, Chebyshev's inequality, random variables- PDF-CDF- Probability Distributions: Binomial, Poisson, Exponential, Uniform, and Normal.

Unit II

Chapter 3: Regression

Introduction to method of least squares, fitting of curvesy=a+bx, $y = ab^x$, correlation and regression. Engineering problems.

Chapter 4: Fourier Series

Complex Sinusoids, Fourier series representations of four classes of signals, Periodic Signals: Fourier Series representations, Derivation of Complex Co-efficients of Exponential Fourier Series and Examples. Convergence of Fourier Series. Amplitude and phase spectra of a periodic signal. Properties of Fourier Series (with proof): Linearity, Symmetry Properties, Time shift, Frequency Shift, Scaling, Time differential differentiation coefficients, Time domain Convolution, Multiplication Theorem, Parseval's theorem and Examples on these properties.

Chapter 6: Fourier Transform

Fourier representation of non-periodic signals, Magnitude and phase spectra. Properties of Fourier Transform: Linearity, Symmetry Properties, Time shift, Frequency Shift, Scaling, Time differential differentiation coefficients, Time domain Convolution, Multiplication Theorem, Parseval's theorem and Examples on these properties.

Unit III

Chapter 6: Random Process:

1. Introduction to Joint Probability Distributions, marginal distribution, joint pdf and cdf, mean, variance, covariance, correlation.
2. Introduction to Random process, stationary process, mean, correlation and covariance function, autocorrelation function, cross correlation, Power spectral Density: properties of the spectral density; Gaussian Process: Properties of Gaussian process.

Text Books

1. Kreyszig E., Advanced Engineering Mathematics, 10th edition, Wiley, 2015
2. Gupta S C and Kapoor V K, Fundamentals of Mathematical Statistics, 11th edition,Sultan Chand & Sons, 2018
3. Walpole and Myers, Probability and Statistics for Engineers and Scientists, 9thedition , Pearson Education India,2013.

Reference Books:

1. Simon Haykin, Barry Van Veen, Signals and SystemsWiley; Second edition ,2007
2. J. Susan Milton, Jesse C. Arnold, Introduction to Probability and Statistics: Principles and Applications for Engineering and the Computing Sciences, 4th edition, TATAMcGraw-Hill Edition, 2017
3. Ian Glover & Peter Grant, Digital Communications, 3rd edition, Pearson 2009.

Back to Semester - III

Program: Electronics Engineering (VLSI Design & Technology)		Semester: III
Course Title: Corporate Communication		Course Code: 22EHSH201
L-T-P: 0.5-0-0	Credits: 0.5	Contact Hours: 1 hrs/week
ISA Marks: 100	ESA Marks: --	Total Marks: 100
Teaching Hours: 16Hrs	Examination Duration: 3 Hrs	

Chapter No. 1. Communication Skills

Tools of Communication, Listening, Body Language, Common Postures and Gestures, Open and Closed Body Language, Body Language to be used in Corporate Scenarios, Voice: Pitch, Pace, and Pause, Verbal Language: Positive & Negative Vocabulary, Corporate Conversations

Chapter No. 2. Presentation Skills

Zero Presentation, Individual Presentations, and feedback, Making Presentations Interactive, Types of Questions, Taking off and Signing off differently, Captivating your Audience, Corporate Presentations

Chapter No. 3. Spoken English

Phonetic and Non-Phonetic Languages, Introduction to IPA, Sounds in English, Syllables, Word Stress, Rhythm, Pausing, and Intonation

Chapter No. 4. Written English

Vocabulary Enhancement Strategies, Root Words in English, Grammar Improvement Techniques, Dictionary Usage, Similar and Contradictory Words

Reference Books:

1. Diana Booher - Communicate With Confidence, Mc Graw Hill Publishers
2. Norman Lewis – Word Power Made Easy, Goyal Publishers
3. Cambridge Advanced Learner’s Dictionary, Cambridge University Press.

Back to Semester - III

Program: Electronics Engineering (VLSI Design & Technology)		Semester: III Semester
Course Title: Circuit Analysis		**Course Code: 23EVTC201**
L-T-P: 4-0-0	**Credits: 4**	**Contact Hours: 4Hrs/week**
ISA Marks: 50	**ESA Marks: 50**	**Total Marks: 100**
Teaching Hours: 50Hrs	**Examination Duration:3 Hrs**	

Unit I

Chapter 1: Basics

Active and passive circuit elements, Voltage & current sources, Resistive networks, Nodal Analysis, Super node, Mesh Analysis, Super mesh, Star – Delta Transformation.
[Text 1: Chapter 4,5, 7]

Chapter 2: Network Theorems

Homogeneity, Superposition and Linearity, Thevenin's & Norton's Theorems, Maximum Power Transfer Theorem, Miller's theorem, Reciprocity principle.
[Text 1: Chapter 5]

Chapter 3: Network topologies

Graph of a network, Concept of tree and co-tree, incidence matrix, tie set and cut set schedules, Formulation of Equilibrium equations in matrix form, Solution of resistive networks.
[Text 1: Chapter 5]

Unit II

Chapter 4: Two Port Networks

Two port variables, Z, Y, H, G, A- Parameter representations, Input and output impedance calculation, Series, Parallel and Cascade network connections, and their (suitable) models.
[Text 2: Chapter 11]

Chapter 5: Time and Frequency domain Representation of Circuits

Order of a system, Concept of Time constant, System Governing equation, System Characteristic equation, Initial conditions, Transfer Functions (Fourier and Laplace domain representation)
[Text 2: Chapter 4]

Chapter 6: First order circuits

Transient response of R-C and R-L networks (with Initial conditions) Concept of phasor, Phasor diagrams, Frequency response characteristics, Polar plots R-C, R-L circuits as differentiator and integrator models, time and frequency domain responses R-C, R-L circuits as Low pass and high pass filters
[Text 2: Chapter 5, Text 1: Chapter 8,9,10]

Unit III

Chapter No. 7. Higher order circuits

Higher order R-C, R-L, and R-L-C networks, time domain and frequency domain representation, Series R-L-C circuit, Transient response, Damping factor, Performance parameters, Quality factor, Frequency response curve, Peaking of frequency curve and its relation to damping factor. Series and Parallel Resonance, Quality factor, Selectivity and Bandwidth

[Text 2: Chapter 7,8] [Text 1: Chapter 4,5, 7]

Text Books

1. W H Hayt, J E Kemmerly, S M Durban, "Engineering Circuit Analysis"McGraw Hill Education; Eighth edition ,2013
2. M E. Van Valkenburg, Network Analysis, Third edition Pearson Education, 2019

Reference Books:

1. Joseph Edminister, Mahmood Nahavi, Electric Circuits, 5th edition, McGraw Hill Education, 2017
2. V. K. Aatre, —Network Theory and Filter Design,3rd edition, New Age International Private Limited,2014

Back to Semester - III

Program: Electronics Engineering (VLSI Design & Technology)		Semester: III Semester
Course Title: Analog Electronic Circuits		Course Code: 23EVTC202
L-T-P: 4-0-0	Credits: 4	Contact Hours: 4Hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 50Hrs	Examination Duration:3 Hrs	

Unit I

Chapter 1: Diode Models and Circuits

Recap of diode models: Exponential model, piece-wise linear model, constant voltage drop model, ideal diode model, small signal diode model and derivation of small signal diode resistance. Applications of diodes as a Clipping and clamping circuits with and without DC bias voltage; Voltage doublers Numericals on applications.
(T1: 2.2, 2.3.1 to 2.3.8, 2.6.1to 2.6.3.)

Chapter 2: Bipolar junction transistors

Recap of DC load line and bias point, small signal operation-the transfer characteristics, the amplifier gain, and operation as a switch. Biasing of BJT: voltage divider, small signal models of bipolar transistors, two port modeling of amplifiers, H-model, ac analysis of BJT circuits-coupling and bypass capacitor, Common emitter circuit analysis without RE resistance (Emitter resistor) Numericals on amplifiers and switch
(T1: 3.2.1,3.2.2, 3.2.3, 3.2.4, 3.3.1, 3.3.2, 3.3.4)

Chapter 3: MOSFETs structure and physical operation

MOSFET Device structure, NMOS :Depletion type ; operation with no gate voltage, positive and negative gate voltage and Enhancement type ; operation with no gate voltage, positive and negative gate voltage creating a channel for current flow, applying small vds, operation as vds is increased, Derivation of threshold voltage of MOSFET, Operating the MOS transistor in the sub threshold region, Pinch off effect , channel length modulation effect , derivation of the ID-VDS relationship, with and without channel length modulation. Finite output resistance (rds on) in saturation, PMOS: Drain and Transfer characteristics, circuit symbol, the ID v/s VDS characteristics, and the role of the substrate-the body effect, temperature effects, breakdown and input protection. Threshold Voltage Derivation MOSFET circuits at DC.

Unit II

Chapter 4: Biasing of MOSFETs

MOSFET circuits at DC continued. Biasing in MOS amplifier circuits: By fixing VGS; By fixing VG; With drain to gate feedback resistor; Constant current source biasing, MOSFET as a switch Large – signal operation, operation as a linear amplifier and Numericals.
(T1:4.3)

Chapter 5: MOSFET amplifiers

Small signal operation and models, single stage MOS amplifiers, the MOSFET internal capacitance, Derivation of CS, CG and CD amplifiers parameters and its comparison, Implications on gain and

Bandwidth. Source degenerated common source amplifier, cascode and cascaded circuits High frequency model of the MOSFET, revision of common-gate, common- source, common-drain circuits; poles and zeros in the transfer function
(T1:4.4,4.5, 4.6.1 to 4.6.7, 4.7.1, 4.7.2, 4.7.3, 4.7.5, 4.7.6, 4.7.7;4.8.1,4.8.2, 4.8.3,4.8.4, 4.9.1 to 4.9.3)

Unit III

Chapter 6: Feedback Amplifiers

General feedback structure (Block schematic), Feedback desensitivity factor, positive and negative feedback Nyquist stability Criterion, RC phase shift oscillator, wein bridge Oscr, merits of negative feedback, feedback topologies: series-shunt feedback amplifier, series-series feedback amplifier, and shunt-shunt and shunt-series feedback amplifier with examples
(T1:7.1 to 7.6)

Chapter 7: Large Signal Amplifiers

Classification of amplifiers: (A, B, AB and C); Transformer coupled amplifier, push-pull amplifier Transistor case and heat sink.
(T1:12.1 to 12.6;12.8.4)

Text Books

1. A.S. Sedra& K.C. Smith, "Microelectronic Circuits",7th edition, Oxford University Press, 2017

Reference Books:

1. JacobMillman and Christos Halkias-Integrated Electronics "McGraw Hill Education, 2nd edition 2017
2. DavidA.Bell,-Electronic Devices and Circuits, Oxford Fifth edition 2008
3. Grey,Hurst,Lewis and Meyer,-Analysis and design of analog integrated circuits,Wiley,5th edition 2009
4. Thomas L.Floyd,-Electronic devices ,Pearson, 10th edition, 2018
5. Richard R. Spencer & Mohammed S. Ghousi, — Introduction to Electronic Circuit Design‖, Pearson Education,2003
6. J. Millman& A. Grabel, "Microelectronics"-2nd edition, McGraw Hill,2017
7. BehzadRazavi,-Fundamentals of Microelectronics, 2nd edition Wiley;2013

Back to Semester - III

Program: Electronics Engineering (VLSI Design & Technology)		Semester: III Semester
Course Title: Digital Circuits		Course Code: 23EVTC203
L-T-P: 4-0-0	Credits: 4	Contact Hours: 4Hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 50Hrs	Examination Duration:3 Hrs	

Unit I

Chapter 1: Logic Families

Logic levels, output switching times, fan-in and fan-out, comparison of logic families

Chapter 2: Principles of Combinational Logic

Definition of combinational logic, canonical forms, Generation of switching equations from truth tables, Karnaugh maps-3,4 variables, Incompletely specified functions (Don't care terms),Simplifying Maxterm equations, Quine-McCluskey minimization technique- Quine-McCluskey using don't care terms, Reduced Prime Implicant Tables.

Chapter 3: Analysis and design of combinational logic

General approach, Decoders-BCD decoders, Encoders, Digital multiplexers- Using multiplexers as Boolean function generators. Adders and subtractors-Cascading full adders, Look ahead carry adders, Binary comparators.

Unit II

Chapter 4: Introduction to Sequential Circuits

Basic Bistable Element, Latches, A SR Latch, Application of SR Latch, A Switch De bouncer, The SR Latch, The gated SR Latch, The gated D Latch, The Master-Slave Flip-Flops (Pulse-Triggered Flip-Flops): The Master-Slave SR Flip-Flops, The Master-Slave JK Flip-Flop, Edge Triggered Flip- Flop: The Positive Edge-Triggered D Flip-Flop, Negative-Edge Triggered D Flip-Flop; Characteristic Equations

Chapter 5: Analysis of Sequential Circuits

Registers and Counters, Binary Ripple Counters, Synchronous Binary counters, Ring and Johnson Counters, Design of a Synchronous counters, Design of a Synchronous Mod-n Counter using clocked JK Flip-Flops Design of a Synchronous Mod-n Counter using clocked D, T or SR Flip-Flops.

Unit III

Chapter No. 6. Sequential Circuit Design

Introduction to Sequential Circuit Design, Mealy and Moore Models, State Machine notations, Synchronous Sequential Circuit Analysis, Construction of state Diagrams and counter design.

Chapter No. 7. Introduction to memories

Introduction and role of memory in a computer system, memory types and terminology, Read Only memory, MROM, PROM, EPROM, EEPROM, Random access memory, SRAM, DRAM, NVRAM.

Text Books

1. Donald D Givone, Digital Principles and Design,McGraw Hill Education ,2017
2. John M Yarbrough, Digital Logic Applications and Design,1st edition Cengage Learning,2006
3. A AnandKumar, Fundamentals of digital circuits 4th Revised edition, PHI ,2016

Reference Books:

1. Charles H Roth, Fundamentals of Logic Design,7th edition, Cengage Learning, 2015
2. ZviKohavi, Switching and Finite Automata Theory Cambridge University Press; 3 edition October 2009
3. R.D. Sudhaker Samuel, Logic Design, Pearson Education ,2010
4. R P Jain, Modern Digital Electronics ,4th edition,McGraw Hill Education,2009

Back to Semester - III

Program: Electronics Engineering (VLSI Design & Technology)		Semester: III Semester
Course Title: Signals and Systems		Course Code: 23EVTC204
L-T-P: 4-0-0	Credits: 4	Contact Hours: 4Hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 50Hrs	Examination Duration:3 Hrs	

Unit I

Chapter 1: Signal Representation

Definition of a signals and systems, classification of signals, (analog and discrete signal, periodic and aperiodic, deterministic and random signals, even and odd signals, energy and power), basic operation on signals (independent variable, dependent variable, time scaling, multiplication, time reversal), elementary signals (Impulse, step, ramp, sinusoidal, complex exponential), Systems Interconnections (series, parallel and cascade), properties of linear systems. (homogeneity, superposition, linearity and time invariance, stability, memory, causality)

Chapter 2: LTI System Representation

Impulse response representation and properties, Convolution, convolution sum and convolution integral. Differential and difference equation Representation, Block diagram representation.

Unit II

Chapter 3: Fourier representation for signals

Introduction, Discrete time Fourier series (derivation of series excluded) and their properties. Discrete Fourier transform (derivation of transform excluded) and properties

Chapter 4: Applications of Fourier transform

Introduction, frequency response of LTI systems, Fourier transform representation of periodic signals, Fourier transform representation of discrete time signals. Sampling of continuous time signals**.**

Unit III

Chapter No. 05: Z-transform

Definition of z-transform, Properties of ROC, Properties of Z-transforms: Inverse z-transforms (Partial Fraction method, long division method), Unilateral Z-transform, Transform of LTI.

Text Books:

1. Simon Haykin and Barry Van Veen, Signals and Systems, 2nd edition Wiley,2007
2. Alan V Oppenheim, Alan S Willsky and S. Hamid Nawab, Signals and Systems, Second, PHI public,1997

Reference Books:

1. H. P Hsu, R. Ranjan, Signals and Systems, 2nd edition, McGraw Hill ,2017
2. GaneshRaoandSatishTunga, SignalsandSystems1st edition, Cengage India, 2017
3. M.J.Roberts, Fundamentals of Signals and Systems 2nd edition, McGraw Hill Education, 2017

Back to Semester - III

Program: Electronics Engineering (VLSI Design & Technology)		Semester: III Semester
Course Title: Digital Circuits Lab		**Course Code: 23EVTP201**
L-T-P: 0-0-1	**Credits: 1**	**Contact Hours: 2Hrs/week**
ISA Marks: 80	**ESA Marks: 20**	**Total Marks: 100**
Teaching Hours: --	**Examination Duration:**	

List of Experiments:

1. Characterization of TTL Gates– Propagation delay, Fan-in, Fan-out and NoiseMargin.
2. To verify of Flipflops (a) JK Master Slave (b) T-type and (c)D-Type
3. Design and implement binary to gray, gray to binary, BCD to Ex-3 and Ex-3 to BCD codeconverters.
4. Design and implement BCD adder and Subtractor using 4 bit paralleladder.
5. Design and implement n bit magnitude comparator using 4- bitcomparators.
6. Design and implement Ring and Johnson counter using shiftregister.
7. Design and implement 8:3 Priority Encoder
8. Design and implement frequency divider
9. Design and implement mod-6 synchronous and asynchronous counters using flip flops.
10. Design and implement given functionality using decodersandmultiplexers.
11. Design and implement a digital system to display a 3-bit counter on a 7-segment display. Demonstrate the results ona general purposePCB**.**

****Note-All above experiments are to be conducted along with simulation.**

Digital Circuits Lab: Simulation of combinational and sequential circuits using netlist based Spice Simulators (Avoid using drag n drop), before implementing the circuits on breadboard

Reference Books:

1. K.A.Krishnamurthy-Digital labprimer||, Pearson Education Asia Publications, 2003.
2. A.P. Malvino, -Electronic Principles 7th edition, McGraw Hill Education,2017

Back to Semester - III

Program: Electronics Engineering (VLSI Design & Technology)		Semester: III Semester
Course Title: Analog Electronic Circuits Lab		**Course Code: 23EVTP202**
L-T-P: 0-0-1	**Credits: 1**	**Contact Hours: 2Hrs/week**
ISA Marks: 80	**ESA Marks: 20**	**Total Marks: 100**
Teaching Hours: --	**Examination Duration:**	

List of Experiments:

1. Study of multi-meters, power supplies, function generators, Oscilloscopes; Identification of various components and devices, e.g. resistors, capacitors, diodes, transistors.
2. Design & analyze Diode Clipping circuits.
3. Design & analyze Positive and Negative Clamping circuits.
4. Study of BJT as a Switch.
5. Study the input and output characteristics of MOSFET.
6. To study the basic current mirror circuit.
7. MOSFET as a source follower (Buffer).
8. Study of transformer-less Class B push pull power amplifier and determination of its conversion efficiency
9. Design an amplifier using BJT and determine its gain, input, output impedance and frequency response of RC Coupled single stage BJT amplifier
10. Design an amplifier using MOSFET and determine its gain, input, output impedance and frequency response of a CS amplifier.
11. Design a regulated power supply for the given specifications

**Note-All above experiments are to be conducted along with simulation.

*Analog Electronic Circuits Lab: Simulation of designed circuits using LTSpice Simulator, before implementing the circuits on breadboard.

Reference Books:

1. “Integrated Electronics”, by Jacob Millman and Christos Halkias, McGraw Hill,
2. "Microelectronic Circuits", by A.S. Sedra & K.C. Smith, 7th Edition, Oxford Univ. Press, 2017.
3. “Electronic Devices and Circuits” by David A. Bell, 4thedition, PHI publication 2007.
4. “Analysis and design of analog integrated circuits,” by Grey, Hurst, Lewis and Meyer, 4thedition.

   Device data sheets.
5. KLETECH Electronics and Communication Engineering Department 2023-24 Analog Electronics Lab manual.

Back to Semester - III

Program: Electronics Engineering (VLSI Design & Technology)		Semester: III Semester
Course Title: Microcontroller Architecture & Programming		Course Code: 23EVTF201
L-T-P: 2-0-1	Credits: 3	Contact Hours: 4Hrs/week
ISA Marks: 80	ESA Marks: 20	Total Marks: 100
Teaching Hours: 40Hrs	Examination Duration: Hrs	

Unit I

Chapter 1: Microprocessors and microcontroller

Introduction, Microprocessors and Microcontrollers, A Microcontroller Survey, RISC & CISC CPU Architectures, Harvard & Von-Neumann CPU architecture.

Chapter 2: The 8051 Architecture

8051 Microcontroller Hardware, Input / Output Pins, Ports and Circuits, semiconductor Memories, Interfacing external RAM & ROM memories.

Chapter 3: Addressing Modes and Arithmetic Operations

Addressing modes, External data Moves, Code Memory, Read Only Data Moves / Indexed Addressing mode, Data exchanges, stack concept and related instructions, example programs. Logical Operations: Introduction, Byte level, logical Operations, Bit level Logical Operations, Rotate and Swap Operations, Example Programs, Arithmetic Operations: Introduction, Flags, Incrementing and Decrementing, Addition, Subtraction Multiplication and Division, Decimal Arithmetic, Example Programs.

Unit II

Chapter 4: Branch operations

Jump Operations: Introduction, The JUMP and CALL Program range, Jump calls and Subroutines Interrupts and Returns,Example Problems.

Chapter 5: 8051 Programming in 'C'

Data Types and Time delays in 8051C, I/O Programming,Logic operations,Data Conversion programs,Accessing code ROM space,. Data serialization.

Chapter 6: Counter/Timer Programming in 8051

Programming 8051 Timers, Programming Timer0 and Timer1 in 8051C

Unit III

Chapter 7: Serial Communication

Basics of Serial Communication, 8051 connections to RS-232,8051 Serial Communication modes, Programming, Serial port programming in C.

Chapter 8: 8051 interfacing and applications

Interfacing 8051 to LCD, Keyboard, ADC, DAC, Stepper Motor, DC Motor.

Chapter 9: Interrupts
Introduction to interrupts, interripts vs polling, classification of inerrupts, inerrupt priority, inerrupt vector table, inerruptt service routine

Text Books

1. "The 8051 Microcontroller Architecture, Programming & Applications" by ' Kenneth J. Ayala', Penram International, 1996
2. "The 8051 Microcontroller and Embedded systems", by ' Muhammad Ali Mazidi and Janice Gillispie Mazidi', Pearson Education, 2003

Reference Books:

1. "Programming and Customizing the 8051 Microcontroller ", by 'Predko', TMH.

Back to Semester - III

KLE Technological University | Creating Value, Leveraging Knowledge

Program: Electronics Engineering (VLSI Design & Technology)		Semester: III Semester
Course Title: C Programming (for Diploma)		Course Code: 23EVTF202
L-T-P: 0-0-2	Credits: 2	Contact Hours: 4 Hrs/week
ISA Marks: 80	ESA Marks: 20	Total Marks: 100
Teaching Hours: 52Hrs	Examination Duration:	

Unit I

1. Write a C program to perform addition, subtraction, multiplication and division of two numbers.
2. Write a C program to
   i) Identify greater number between two numbers using C program.
   ii) To check a given number is Even or Odd.
3. Write a C program to
   i) To find the roots of a quadratic equation.
   ii) Find the factorial of given number.
4. Write a C program to
   i) To find the sum of n natural numbers.
   ii) Print the sum of 1 + 3 + 5 + 7 + + n
5. Write a C program to
   i) Print the pattern.

```
*
* *
* * *
* * * *
* * * * *
```

   ii) Print the pattern

```
1
1 2
1 2 3
1 2 3 4
1 2 3 4 5
```

6. Write a C program to
   To test whether the given character is Vowel or not. (using switch case)
7. Write a C program to
   To accept 10 numbers and make the average of the numbers using one dimensional array.
8. Write a C program to
   Find out square of a number using function.
9. Write a C program to
   To find the summation of three numbers using function.
10. Write a C program to
    Find out addition of two matrices.

Text Books

1. Programming in ANSI C, E Balagurusamy.

Back to Semester - III

Program: Electronics Engineering (VLSI Design & Technology)		Semester: IV Semester
Course Title: Linear Algebra and Partial Differential Equations		Course Code: 15EMAB208
L-T-P: 4-0-0	Credits: 4	Contact Hours: 4Hrs/Week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 50Hrs	Examination Duration:3 Hrs	

Unit I

Chapter 1: Partial differential equations

Introduction, classification of PDE, Formation of PDE, Solution of equation of the type Pp + Qq = R, Solution of partial differential equation by direct integration methods, method of separation of variables. Modeling: Vibration of string-wave equation, heat equation. Laplace equation. Solution by method of separation of variables.

Chapter 2: Finite difference method

Finite difference approximations to derivatives, finite difference solution of parabolic PDE, explicit and implicit methods; Hyperbolic PDE-explicit method, Elliptic PDE-initial-boundary Value problems.

Unit II

Chapter 3: Fourier Series

Complex Sinusoids, Fourier series representations of four classes of signals, Periodic Signals: Fourier Series representations, Derivation of Complex Co-efficients of Exponential Fourier Series and Examples. Convergence of Fourier Series. Amplitude and phase spectra of a periodic signal. Properties of Fourier Series (with proof): Linearity, Symmetry Properties, Time shift, Frequency Shift, Scaling, Time differential differentiation coefficients, Time domain Convolution, Multiplication Theorem, Parseval's theorem and Examples on these properties.

Chapter 4: Fourier Transform

Fourier representation of non-periodic signals, Magnitude and phase spectra. Properties of Fourier Transform: Linearity, Symmetry Properties, Time shift, Frequency Shift, Scaling, Time differential differentiation coefficients, Time domain Convolution, Multiplication Theorem, Parseval's theorem and Examples on these properties.

Unit III

Chapter5: Complex analysis

Function of complex variables. Limits, continuity and differentiability. Analytic functions, C-R equations in Cartesian and polar forms, construction of Analytic functions (Cartesian and polar forms).

Chapter 6: Complex Integration

Line integral, Cauchy's theorem- corollaries, Cauchy's integral formula. Taylor's and Laurent Series, Singularities, Poles, Residue theorem – problems.

Text Books

1. Simon Haykin, Barry Van Veen, Signals and Systems,2nd edition, Wiley,2007
2. Peter V. O'neil, Advanced Engineering MathematicsCengage Learning Custom Publishing; 7th Revised edition2011
3. DennisGZillandMichaelRCullin, "Advanced Engineering Mathematics",4th edition, NarosaPublishingHouse,NewDelhi,2012

Reference Books:

1. Kreyszig E., Advanced Engineering Mathematics,10th edition, Wiley,2015
2. Stanley J Farlow, Partial differential equations for Scientists and Engineers, Dover publications, INC, New York,1993

Back to Semester - IV

Program: Electronics Engineering (VLSI Design & Technology)		Semester: IV
Course Title: Problem Solving & Analysis		Course Code: 22EHSH202
L-T-P: 0.5-0-0	Credits: 0.5	Contact Hours: 1 hrs/week
ISA Marks: 100	ESA Marks: --	Total Marks: 100
Teaching Hours: 16Hrs	Examination Duration: 3 Hrs	

Chapter No. 1. Analytical Thinking

Analysis of Problems, Puzzles for practice, Human Relations, Direction Tests; Looking for Patterns: Number and Alphabet Series, Coding Decoding; Diagrammatic Solving: Sets and Venn diagram-based puzzles; Visual Reasoning, Clocks and Calendars

Chapter No. 2. Mathematical Thinking

Number System, Factors and Multiples, Using Simple Equations for Problem Solving, Ratio, Proportion, and Variation

Chapter No. 3. Verbal Ability

Problem Solving using Analogies, Sentence Completion

Chapter No. 4. Discussions & Debates

Team efforts in Problem Solving; A Zero Group Discussion, Mock Group Discussions, and Feedback; Discussion v/s Debate; Starting a Group Discussion: Recruitment and other Corporate Scenarios; Evaluation Parameters in a Recruitment Group Discussion, Types of Initiators: Verbal and Thought, Conclusion of a Discussion

Reference Books:

1. R. S. Aggarwal, “A Modern Approach to Verbal and Non – Verbal Reasoning”, Sultan Chand and Sons, New Delhi, 2018
2. R. S. Aggarwal, “Quantitative Aptitude”, Sultan Chand and Sons, New Delhi, 2018
3. Chopra, “Verbal and Non – Verbal Reasoning”, MacMillan India
4. M Tyra, “Magical Book on Quicker Maths”, BSC Publications, 2018
5. Diana Booher - Communicate With Confidence, Mc Graw Hill Publishers
6. Norman Lewis–Word Power Made Easy, Goyal Publishers
7. Cambridge Advanced Learner’s Dictionary, Cambridge University Press.
8. Kaplan’s GRE guide

Back to Semester - IV

Program: Electronics Engineering (VLSI Design & Technology)		Semester: IV Semester
Course Title: Semiconductor Device Physics		Course Code: 23EVTC205
L-T-P: 3-0-0	Credits: 3	Contact Hours: 3Hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 40Hrs	Examination Duration:3 Hrs	

Unit I

Chapter 1. Energy Band Model

Energy bands in solids - Intrinsic and Extrinsic semiconductors - Direct and Indirect bandgap -Density of states - Fermi distribution -Free carrier densities - Boltzmann statistics - Thermal equilibrium.

Chapter 2. Motion and Recombination of Electrons and Holes

Current flow mechanisms: Drift current, Diffusion current - Mobility of carriers - Current density equations - Continuity equation

Chapter 3. PN and Metal–Semiconductor Junctions

Thermal equilibrium physics - Energy band diagrams - Space charge layers - Poisson equation - Electric fields and Potentials - p-n junction under applied bias - Static current-voltage characteristics of p-n junctions - Breakdown mechanisms.

Unit II

Chapter 4. MOS Capacitor

Accumulation - Depletion - Strong inversion - Threshold voltage - Contact potential - Gate work function - Oxide and Interface charges - Body effect - C-V characteristics of MOS.

Chapter 5. MOS Transistor

Drain current - Saturation voltage - Sub-threshold conduction - Effect of gate and drain voltage on carrier mobility - Compact models for MOSFET and their implementation in SPICE: Level 1, 2 and 3 - MOS model parameters in SPICE.

Unit III

Chapter 6. MOSFETs in ICs—Scaling, Leakage, and Other Topics

Effect of scaling - Channel length modulation - Punch-through - Hot carrier degradation - MOSFET breakdown - Drain-induced barrier lowering

Chapter 7.

Effect of tox - Effect of high-k and low-k dielectrics on the gate leakage and Source and drain leakage - tunneling effects - Different gate structures in UDSM - Impact and reliability challenges in UDSM

Text Books

1. Chenming Hu, Modern Semiconductor Devices for Integrated Circuit, Pearson education
2. S M Sze, Physics of Semiconductor devices, Wiley Online Library
3. J.P. Colinge and C. A. Colinge, Physics of Semiconductor Devices, Kluwer Academic Publishers, US, 2017
4. M K Achutan and K N Bhatt, Fundamental of Semiconductor Devices, McGraw Hill Education, US, 2017

Back to Semester - IV

Program: Electronics Engineering (VLSI Design & Technology)		Semester: IV Semester
Course Title: Linear Integrated Circuits		Course Code: 23EVTC206
L-T-P: 4-0-0	Credits: 4	Contact Hours: 4Hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 50Hrs	Examination Duration:3 Hrs	

Unit I

Chapter 1: Current Mirrors

Current Mirror circuits and Modeling, Figures of merit (output impedance, voltage swing), Widlar, Cascode and Wilson current Mirrors, Current source and current sink.

Chapter 2: Basic Op-Amp architecture

Basic differential amplifier, Common mode and difference mode gain, CMRR, 5-pack differential amplifier with design, 7-pack operational amplifier.

Chapter 3: Op-Amp characteristics

Ideal and non-ideal Op-Amp terminal characteristics, Input and output impedance, output Offset voltage, Small signal and Large signal bandwidth.

Unit II

Chapter 4: Op-Amp with Feedback

Op-Amp under Positive and Negative feedback, Impact Negative feedback on Bandwidth, Input and Output impedances, Offset voltage under negative feedback, Follower property & Inversion Property under linear mode operation.

Chapter 5: Linear applications of Op-Amp

DC and AC Amplifier, Summing, Scaling and Averaging amplifiers (Inverting, Non-inverting and Differential configuration), Instrumentation Amplifier, Integrator, Differentiator,Voltage sources, current sources and current sinks, Active Filters –First and second order Low pass & High pass filters. V to I and I to V converters**.**

Unit III

Chapter 6: Nonlinear applications of Op-Amp

Crossing detectors (ZCD. Comparator), Inverting Schmitt trigger circuits, Triangular/rectangular wave generators, Waveform generator, Voltage controlled Oscillator, sample and hold circuits, Phase shift oscillator, Wein bridge oscillator.

Data Converters: Digital to Analog Converters: Weighted resistor; R -2R, Current steering DAC, Pipeline. Analog to Digital Converters: Flash, Dual slope, Pipeline and SAR.

Text Books

1. Behzad Razavi, Design of Analog CMOS Integrated Circuits McGraw-Hill, 2nd edition, 2016

2. Phillip E. Allen, Douglas R. Holberg, CMOS Analog Circuit Design, Oxford University Press, USA, 2010
3. Ramakant A. Gayakwad, Op - Amps and Linear Integrated Circuits, 4th Edition

Reference Books:

1. A.S. Sedra & K.C. Smith, Microelectronic Circuits, 7th Edition, 2017
2. Design With Operational Amplifiers and Analog Integrated Circuits, Sergio Franco, 4th edition, Tata McGraw Hill 2014
3. David A. Bell, Operational Amplifiers and Linear IC's, 3rd ed., Oxford University Press, 2011
4. B. Razavi, Fundamentals of Microelectronics, 2nd edition.

Back to Semester - IV

Program: Electronics Engineering (VLSI Design & Technology)		Semester: IV Semester
Course Title: Computer Architecture		Course Code: 23EVTC207
L-T-P: 2-0-1	Credits: 3	Contact Hours: 4Hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 30Hrs	Examination Duration:3 Hrs	

Unit I

Chapter No. 1: Instructions Representation and Arithmetic for Computers

Representing Instructions in the Computer, Parallelism and Instructions: Synchronization, Translating and Starting a Program, Addition and Subtraction, Multiplication, Division, Floating Point.

[Text 1: Chapter 2,3]

Exercises.

Chapter No. 2: The Processor

Introduction, Logic Design Conventions, Building a Datapath, An overview of pipelining, Pipelined datapath and control, Data Hazards: Forwarding versus Stalling, Control hazards, Exceptions, Parallelism and advanced instruction level parallelism.

[Text 1: Chapter 4]

Case study and Exercises.

Unit II

Chapter No. 3: Large and Fast: Exploiting Memory Hierarchy

Introduction, The Basics of Caches, Measuring and Improving Cache Performance, Virtual Memory, Parallelism and memory hierarchy: cache coherence.

[Text 1: Chapter 5]

Case study and Exercises.

Chapter No. 4: Storage and Other I/O Devices

Introduction, Dependability, Reliability and Availability, Disk Storage, Flash storage, Connecting Processors, Memory, and I/O Devices, Interfacing I/O Devices to the Processor, Memory and Operating System.

[Text 1: Chapter 6]

Unit III

Chapter No. 5: Multicores, Multiprocessors and Clusters

Introduction, Difficulty of creating parallel processing programs, Shared memory multiprocessors Clusters and other message passing multiprocessors, Hardware multithreading, SISD, MIMD, SIMD, SPMD, and vector, Introduction to graphics processing units, Introduction to multiprocessor network topologies, Multiprocessor benchmarks.

[Text 1: Chapter 7]

Text Books

1. Computer Organization and Design, The hardware/Software interface, ARM edition– David A. Patterson, John L.Hennessy. 4th edition, MK publishers,2009

Reference Books:

1. Computer Architecture and Organization– John P. Hayes, 3rd edition, McGraw-Hill, 1998
2. Computer Organization – V. Carl Hamacher, 6th edition, McGraw-Hill Higher Education

Experiment wise plan

List of Experiments planned to meet the requirements of the course

Expt. No.	Experiment Details
	Implement the following arithmetic operations on ARM/FPGA platform.
1	Addition algorithm.
2.	Subtraction algorithm.
3.	Multiplication algorithm.
4.	Division algorithm.
5.	Floating point algorithm.
6.	Introduction to LEGv8 Simulator.
7.	Data Path activity in 3 stage pipeline involving data processing instructions (Single cycle execution).
8.	Data Path activity in 3 stage pipeline involving memory instructions (Multi cycle execution).
9.	Data Path activity in 3 stage pipeline involving I/O related instructions.
10.	Exercise on data hazards.
11.	Exercise on Structural hazards.
12.	Exercise on control hazards.

Back to Semester - IV

Program: Electronics Engineering (VLSI Design & Technology)		Semester: IV Semester
Course Title: ARM Processor & Applications		Course Code: 23EVTC210
L-T-P: 3-0-1	Credits: 4	Contact Hours: 5Hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 40Hrs	Examination Duration:3 Hrs	

Unit I

Chapter No. 1 ARM Architecture

The Acorn RISC machine, Architectural inheritance, Architecture of ARM7TDMI, ARM programmers model, ARM development tools, 3 stage pipeline ARM organization, ARM instruction execution.

Chapter No. 2 Introduction to ARM instruction set

Data processing instruction, Branch instruction, Load store instruction, Software interrupt instruction, Program status register instruction, Conditional execution, Example programs, introduction to thumb instruction and implementation

Chapter No. 3 Assembler rules and Directives

Introduction, structure of assembly language modules, Predefined register names, frequently used directives, Macros, Miscellaneous assembler features. Example programs.

Unit II

Chapter No. 4 Exception handling

Introduction, Interrupts, error conditions, processor exception sequence, the vector table, Exception handlers, Exception priorities, Procedures for handling exceptions.

Chapter No. 5 Introduction to Bus protocols:

I2C, SPI, AMBA (advanced memory bus architecture): AHB, APB

Chapter No. 6 LPC 2148 Controller Architectural overview and GPIO programming

LPC2148 architectural overview, Registers, GPIO Programming: LED, LCD, Seven segment, Stepper Motor, DC Motor, Buzzer, Switch, Keypad.

Unit III

Chapter No. 7 On-chip programming techniques using LPC 2148 Controller

ARM interfacing techniques and programming: Timers, RTC, UART, ADC, DAC, I2C and External Interrupt.

Chapter No. 8 Architectural support for high level languages

Abstraction in software design, data types, floating point data types, The ARM floating point architecture, use of memory, run time environment.

Text Books:

1. Steve Furber, ARM System- on-Chip Architecture, 2nd, LPE, 2002

2. William Hohl, ARM Assembly Language fundamentals and Techniques, 1st, CRC press, 2009

Reference Books:

1. "ARM system Developer's Guide"- Hardbound, Publication date: 2004 Imprint: MORGAN KAUFFMAN
2. User manual onLPC21XX.

List of Experiments	
1	Write an ALP to achieve the following arithmetic operations: i. 32 bit addition ii. 64 bit addition iii. Subtraction iv. Multiplication v. 32 bit binary divide Apply suitable machine dependent optimization technique and analyze for memory and time consumed
2	Write an ALP for the following using loops: i. Find the sum of 'N' 16 bit numbers ii. Find the maximum/minimum of N numbers iii. Find the factorial of a given number with and without look up table. Apply suitable machine dependent optimization technique and analyze for memory and time consumed
3	Write an ALP to i. Find the length of the carriage return terminated string. ii. Compare two strings for equality. Apply suitable machine dependent optimization technique and analyze for memory and time consumed
4	Write an ALP to pass parameters to a subroutine to find the factorial of a number or prime number generation.

	Apply suitable machine dependent optimization technique and analyze for memory and time consumed
5	Write a C program to test working of LEDs and seven segment using LPC2148.
6	Write a C program & demonstrate an interfacing of Alphanumeric LCD 2X16 panel and 4X4 keypad to LPC2148 Microcontroller.
7	Write an ALP to generate the following waveforms of different frequencies i. Square wave ii. Triangular iii. Sine wave
8	Write a program that converts the data read from sensor to a data understandable for the ARM microcontroller
9	Develop a C program to demonstrate the concept of serial communication with an example.
10	Develop an application code using embedded C to accept asynchronous inputs and control the connected device
11	Develop an application code using synchronous communication protocol to display the RTC value on a display device.

Back to Semester - IV

Program: Electronics Engineering (VLSI Design & Technology)		Semester: IV Semester
Course Title: Digital IC Design		**Course Code: 23EVTC209**
L-T-P: 2-0-1	**Credits: 3**	**Contact Hours: 4Hrs/week**
ISA Marks: 80	**ESA Marks: 20**	**Total Marks: 100**
Teaching Hours: 30Hrs	**Examination Duration:2 Hrs**	

Chapter No. 1:
Introduction to VLSI Design flow, Architecture of FPGA, Verilog Language Features, Verilog Operators, Verilog description styles, Verilog Modeling examples, Blocking/Non-Blocking, User defined Primitives.

Chapter No. 2: Sequential Modeling
Sequential Statements, Tasks and Functions, Modeling Finite Sate Machines, Modeling Counters, Data path and Controller Design, Pipelining.

Chapter No. 3: Algorithm to efficient architecture
Efficient Adder Architecture, Efficient Multiplier Architecture, Squaring Circuit Design

Chapter No. 4: Interfacing and pplications
LCD, 7 Segment display, Keyboard, Traffic light controller, Stepper Motor, DC Motor.

Chapter No. 5: Timing Analysis
Timing Analysis Basics, timing issues in digital IC design

Text Books

1. Nazeih M. Botros, HDL Programming –Verilog, Dreamtech Press,2006.
2. J.Bhaskar, “AVerilog Primer“,; 3rd edition, Pearson Education India ,2015

Reference Books:

1. SamirPalnitkar, -Verilog HDL||, PearsonEducation,2ndEdition,2003.
2. Thomas and Moorby, -TheVerilogHardwareDescriptionLanguage||,kluweracademic publishers,5thedition, 2002.
3. StephenBrownandZvonkoVranesic, -Fundamentals ofLogicDesign with Verilog; 2nd edition, McGraw Hill Education 2017.
4. Charles.H.Roth, Jr.,LizyKurianJohn-Digital System DesignusingVHDL||,Thomson, 2ndEdition,2008.

Back to Semester - IV

Program: Electronics Engineering (VLSI Design & Technology)		Semester: IV Semester
Course Title: LIC Lab		**Course Code: 23EVTP203**
L-T-P: 0-0-1	**Credits: 1**	**Contact Hours: 2Hrs/week**
ISA Marks: 80	**ESA Marks: 20**	**Total Marks: 100**
Teaching Hours: --	**Examination Duration: 2 Hrs**	

List of Experiments:

1. To illustrate the functionality and the input-output relationships for the following basic signal conditioning circuits (Linear applications)
   a) Inverting Amplifier
   b) Non-Inverting Amplifier using OP AMP.
2. To implement and study non-linear application of Op-Amp - Precision Rectifier
3. Design & analyze Inverting Schmitt Trigger.
4. Design and realize the performance of inverting and non-inverting Summing amplifier.
5. Implement and study of V-I converters.
6. Realize Integrator and Differentiator for a given input frequency.
7. Realize and verify the performance of Wein-Bridge Oscillator using op-amp
8. Design and realize the frequency responses of 2nd order, Low pass and High pass filter.
9. Realize the following data converters to determine their respective performance parameters.
10. 4-bit R-2R D-A Converter.
11. To verify the electrical parameters of µA 741IC Op-amp.

**Note-All above experiments are to be conducted along with simulation.

* Data Acquisition and Controls Laboratory: Simulation of designed circuits using LTSpice or Proteus Simulator, before implementing the circuits on breadboard.

Reference Books

1. Books/References:
   a. Ramakant Gayakwad, Operational Amplifiers and Linear Integrated Circuits, PHI 4ed.,
   b. Sergio Franco Design with Op-amps and Analog Integrated circuits. Tata McGraw Hill, 3ed.,
   c. Dan Sheingold Analog to Digital Conversion Hand Book, PH, 1986.
   d. David A. Bell, Operational Amplifiers and Linear IC's, 2ed., PHI/Pearson, 2004
   e. Manual: Lab manual prepared by SoECE Department.

Back to Semester - IV

Program: Electronics Engineering (VLSI Design & Technology)		Semester: IV Semester
Course Title: Data Structures Application Lab		**Course Code: 23EVTF203**
L-T-P: 0-0-2	**Credits: 2**	**Contact Hours: 4Hrs/week**
ISA Marks: 80	**ESA Marks: 20**	**Total Marks: 100**
Teaching Hours: --	**Examination Duration:2 Hrs**	

Unit I

Chapter No 1. Analysis of algorithms:

Introduction, Asymptotic notations and analysis, Analysis of recursive and non-recursive algorithms, master's theorem, complexity analysis of algorithms.

Chapter No 2. Analysis of linear data-structures and its applications:

Complexity analysis of basic data structures (Stacks, Queues, Linked lists)

Unit II

Chapter No 3. Analysis of non-linear data-structures and its applications

Trees and applications: Computer representation, Tree properties, Binary Tree properties, Binary search trees properties and implementation, Tree traversals, AVL tree.

Graphs and applications: Computer representation, Adjacency List, Adjacency Matrix, Graph properties, Graph traversals.

Hashing and applications: Hashing, Hash function, Hash Table, Collision resolution techniques, Hashing Applications

Text Books

1. Richard F. Gilberg & Behrouz A. Forouzan, Data Structures A Pseudocode Approach with C, Second Edition.
2. Aaron M. Tenenbaum, Data Structures Using C.

Back to Semester - IV

Program: Electronics Engineering (VLSI Design & Technology)		Semester: IV Semester
Course Title: Data Structures Lab (Dip)		Course Code: 23EVTF204
L-T-P: 0-0-3	Credits: 3	Contact Hours: 6Hrs/week
ISA Marks: 80	ESA Marks: 20	Total Marks: 100
Teaching Hours: --	Examination Duration:2 Hrs	

List of experiments/jobs planned to meet the requirements of the course.

c		Total Weightage: 0.00		No. of lab sessions: 6.00
Expt./ Job No.	**Experiment / Job Details**	**No. of Lab Session(s) per batch (estimate)**	**Marks / Experiment**	**Correlation of Experiment with the theory**
1	Programs on Pointer concepts.	2.00	0.00	
	Learning Objectives : *The students should be able to* Perform basic programming structures on 1. Pointers concepts. 2. 1D and 2Darrays. 3. Pointers to functions. 4. Memory management functions			1
2	Programs on string handling functions, structures union And bit-files.	2.00	0.00	
	Learning Outcomes: *The students should be able to write programs to:* a)Perform string handling functions like 1. String length. 2. String concatenate. 3. Strings compare. 4. String copy.			1

	5. Strings reverse. b) Implement Structures, union and bit-field			
3	Programming on files.	2.00	0.00	
	Learning Outcomes: *The students should be able to write a modular program to:* 1. Open and Close the file. 2. Read and Write the file. 3. Append the file.			1
Category: Exercise		**Total Weightage: 20.00**		**No. of lab sessions: 12.00**
Expt./ Job No.	**Experiment / Job Details**	**No. of Lab Session(s) per batch (estimate)**	**Marks / Experiment**	**Correlation of Experiment with the theory**
4	Programs on implementation of stacks and its applications.	2.00	3.00	
	Learning Outcomes: *The students should be able to:* 1. Write a program to Insert delete and display stack elements for an application. 2. Write a program using stack to convert from Infix to postfix & Infix to Prefix 3. Write a program using stack data structure for base conversion.			3
5	Programs on implementation of different queue data structures.	2.00	4.00	
	Learning Outcomes: *The students should be able to:* Write a program using queue data structure for an application.			3
6	Programs on implementation of different types of Linked lists	2.00	4.00	
	Learning Outcomes:			4

	The students should be able to write a modular program to use the linked lists for an application 1. Insert , delete and display a node in SLL. 2. Insert , delete and display a node in DLL. 3. Insert delete and display a node in CLL.			
7	Programs on Implementation of trees.	2.00	3.00	
	Learning Outcomes: *The students should be able to write modular programs to :* 1. Perform various operations on binary trees. 2. To find max, min value in a binary search trees. 3. To find the height of a tree, 4. To count nodes in a tree. 5. To delete a node in a tree			5
8	Programs to implement different sorting techniques.	2.00	3.00	
	Learning Outcomes: *The students should be able to:* Write modular program on perform the following sorting techniques 1. Selection 2. Insertion 3. Bubble 4. Merge 5. Quick 6. Heap			5
9	Programming on hash tables	2.00	3.00	
	Learning Outcomes: *The students should be able to*			6

	Write modular program on 1. Direct-address tables 2. Hash tables	
	Books/References: 2. Aaron M. Tenenbaum, et al, "Data Structures using C", PHI, 2006 3. Cormen, Leiserson, Rivest " Introduction to Algorithms", PHI, 2001 4. E Balaguruswamy, "The ANSI C programming Language", 2ed., PHI, 2010. 5. YashavantKanetkar, "Data Structures through C", BPB publications 2010 6. Horowitz, Sahani, Anderson-Feed, "Fundamentals of Data Structures in C", 2ed,Universities Press, 2008 7. Richard F. Gilberg, Behrouz A. Forouzan "Data Structures: A Pseudocode Approach With C", 2nd Edition , Course Technology, Oct 2009. 8. Kernighan and Ritchie, The ANSI C programming Language, 2 ed., PHI. 9. Robert Kruse, Data Structures and Program Design in C, 2 ed., Pearson	

Back to Semester - IV

Program: Electronics Engineering (VLSI Design & Technology)		Semester: V Semester
Course Title: CMOS VLSI Design		**Course Code: 24EVTC301**
L-T-P: 4-0-0	**Credits: 4**	**Contact Hours: 4Hrs/week**
ISA Marks: 50	**ESA Marks: 50**	**Total Marks: 100**
Teaching Hours: 50Hrs	**Examination Duration:3 Hrs**	

Unit I

Chapter No. 1: Electronic Analysis of CMOS logic gates

DC transfer characteristics of CMOS inverter, Beta Ratio Effects, Noise Margin, MOS capacitance models. Transient Analysis of CMOS Inverter, NAND, NOR and Complex Logic Gates, Gate Design for Transient Performance, Switch-level RC Delay Models, Delay Estimation, Elmore Delay Model, Power Dissipation of CMOS Inverter, Transmission Gates & Pass Transistors, Tristate Inverter.

Chapter No. 2: Design of CMOS logic gates

Stick Diagrams, Euler Path, Layout design rules, DRC, Circuit extraction, Layout of AOI and OAI circuits, Latch up – Triggering Prevention

Unit II

Chapter No. 3. Designing Combinational Logic Networks

Gate Delays, Driving Large Capacitive Loads, Delay Minimization in an Inverter Cascade, Logical effort. Pseudo nMOS, Clocked CMOS, Dynamic CMOS Logic Circuits, Dual-rail Logic Networks: CVSL, CPL.

Chapter No. 4. Sequential CMOS Circuit Design

Sequencing static circuits, Circuit design of latches and flip-flops, Clocking- clock generation, clock distribution.

Unit III

Chapter No. 5. Adders and Multipliers

Inverting adder, Carry Save Adder, Carry Select adder, Array Multiplier, Carry Save Multiplier and Signed Multiplication.

Chapter No. 6. Introduction To Asic's

Types of ASICs - Design flow - CMOS transistors, CMOS Design rules, Combinational Logic Cell, Sequential logic cell, Data path logic cell, Library cell design, Library architecture.

Text Books

1. John P. Uyemura, Introduction to VLSI Circuits and Systems, 1, Wiley, 2007
2. Neil Weste, David Harris & Ayan Banerjee, CMOS VLSI Design, 3, Pearson Ed, 2005
3. Sung-Mo Kang & Yusuf Leblebici, CMOS Digital Integrated Circuits: Analysis and Design, 3, Tata McGra, 2007

4. M. J. S. Smith, "Application Specific Integrated Circuits", Addison -Wesley Longman Inc., 1997.

Reference Books:

1. FinFET Modeling for IC Simulation and Design: Using the BSIM-CMG Standard By Yogesh Singh Chauhan, Darsen Duane Lu, Vanugopalan Sriramkumar, Sourabh Khandelwal, Juan Pablo Duarte, Navid Payvadosi, Ai Niknejad, Chenming Hu, Elsevier Publication, 2015
2. Wayne, Wolf, Modern VLSI design: System on Silicon, 3, Pearson Ed, 2005
3. Douglas A Pucknell and Kamran Eshraghian, Basic VLSI Design, 3, PHI, 2005
4. Faranak Nekoogar, "From ASICs to SOCs: A Practical Approach", Prentice Hall PTR, 2003.

Back to Semester - V

Program: Electronics Engineering (VLSI Design & Technology)		Semester: V Semester
Course Title: Control Systems		**Course Code: 24EVTC302**
L-T-P: 4-0-0	**Credits: 4**	**Contact Hours: 4Hrs/week**
ISA Marks: 50	**ESA Marks: 50**	**Total Marks: 100**
Teaching Hours: 50Hrs	**Examination Duration:3 Hrs**	

Unit I

Chapter No. 1. Control System Representation

Concepts of Control Systems- Open Loop And Closed Loop Control Systems, Feedback characteristics, Examples, System representation: Differential Equations, Transfer function, Impulse response, System Modeling: Electrical Mechanical, Rotational Mechanical Systems.

Chapter No. 2. Block Diagram And Signal Flow Graphs

Transfer Functions, Block Diagram Algebra and Representation by Signal Flow Graph - Reduction Using Mason's Gain Formula.

Chapter No. 3. Time Response Analysis

Standard Test Signals (impulse, step, ramp, parabola)-Order and Type of System, Time Response of First Order Systems – Characteristic Equation of Feedback Control Systems, Transient Response of Second Order Systems - Time Domain Specifications – Steady State Response - Steady State Errors and Error Constants – Effects Of Proportional Derivative, Proportional Integral Systems

Unit II

Chapter No. 4. Stability Analysis In S-Domain

The Concept of Stability (BIBO, all system poles on LHS, Impulse response is convergent, Marginal stability- necessary conditions) – Routh's Stability Criterion – Limitations of Routh's Stability Criterion (Applications only). Root Locus Technique: The Root Locus Concept - Construction of Root Loci.

Chapter No. 5. Frequency Response Analysis

Introduction, Bode Diagrams-Determination of Frequency Domain Specifications and Transfer Function from The Bode Diagram-Phase Margin And Gain Margin-Stability Analysis From Bode Plots**.**

Unit III

Chapter No. 6. Stability Analysis In Frequency Domain

Polar Plots, Nyquist Plots Stability Analysis, Assessment of Relative Stability Using Nyquist Criterion.

Chapter No. 7. Introduction to Controller Design

The Design Problem. Preliminary Consideration of Classical Design, Realization Of Basic Compensators (Lag, Lead and dominant pole compensation), P, I, PI, PD & PID Controllers.

Text Books

1. J. Nagrath and M. Gopal, Control Systems Engineering; Sixth edition, New Age International PvtLtd 2018
2. B. C. Kuo, Automatic Control Systems, 9th edition, John wiley and Sons,2014

Reference Books:

1. Katsuhiko Ogata, Modern Control Engineering, 5th edition, Pearson education India Pvt. Ltd,2015,
2. Richord C Dorf and Robert H. Bishop, Modern Control Systems, 13th edition, Pearson; 2016

Back to Semester - V

Program: Electronics Engineering (VLSI Design & Technology)		Semester: V Semester
Course Title: Machine Learning & Deep Learning		Course Code: 24EVTC303
L-T-P: 2-0-2	Credits: 4	Contact Hours: 6Hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 30Hrs	Examination Duration: 3 Hrs	

Unit I

Chapter No.1 Introduction

Motivation, History and Evolution, Definition (ETP, Examples), Types of Machine Learning: Supervised, Unsupervised and Reinforcement learning.

Chapter No. 2 Supervised Learning

Model Representation: Basic Terminologies (Variable/features, Input, Output, Model, Learning Algorithm, Hypothesis, Cost/Loss function) Linear Regression: Single Variable (Representation of hypothesis, cost function, Optimization: Sum of squared error (L1 and L2), parameters/weights, bias) without bias and with bias. Model Optimization: Introducing Iterative optimization (Sum of squares error function, Gradient descent algorithm) and non-iterative optimization. Linear Regression: Polynomial Regression and Multi-variable Regression (Representation of hypothesis, cost function, Optimization).Model Optimization: Gradient descent algorithm (Learning rate/ step size, Normalization/ Feature Scaling).Model Optimization: Non-iterative optimization (Normal Equation).Logistic Regression: Hypothesis Representation, Decision boundary, Cost function, Logistic Regression: Optimization (Gradient Descent), Multi-class classification (One-vs.-all classification using logistic regression), Classical supervised learning algorithm- Support Vector Machine (SVM).

Chapter No. 3 Performance Evaluation

Performance Evaluation of learning models:Metrics (Confusion matrix, Precision, Recall, F1 Score, RoC curves), Modeling data and validating learning, Over fitting, Trade of Bias and Variance, Methods to overcome over fitting (Feature reduction, Regularization).

Unit II

Chapter No. 4 Unsupervised Learning Clustering:

Introduction, K-means Clustering, Algorithm, Cost function, Applications, Dimensionality Reduction: Motivation, Definition, Methods of Dimensionality reduction, Dimensionality Reduction: PCA-Principal Component Analysis.

Chapter No. 5 Introduction to Neural Network and deep learning:

Introduction to Neural Networks (Motivation: non-linear model, Neurons and perception), Model representation: Neural Network Architecture (Activation units, Layers), Neural Network: Initialization, Forwards propagation, and Cost function, Back propagation algorithm, Multi-class classification, Steps to train a neural network, Applications of Neural Networks, Introduction to Deep Learning (Motivation, Overview), Convolution Neural Networks (CNN) (Architecture, terminologies, Evolution and Modelling).

Unit III

Chapter No. 6 Deep learning algorithms

Recurrent Neural Networks (RNN), Self-supervised models (Auto encoders and variants), Generative Models (GAN, its variants and applications).

Chapter No. 7 Sequence to Sequence Learning:

Attention networks, Transformer based architecture, Transformer for Time-Series

Text Books

1. Tom Mitchell, Machine Learning, 1, McGraw-Hill, 1997
2. Christopher Bishop, Pattern Recognition and Machine Learning, 1, Springer, 2007

Reference Books:

1. Trevor Hastie, Robert Tibshirani, Jerome Friedman, The Elements of Statistical Learning: Data Mining Inference and Prediction, 2, Springer, 2009

Back to Semester - V

Program: Electronics Engineering (VLSI Design & Technology)		Semester: V Semester
Course Title: Electromagnetic Fields and Waves		Course Code: 24EVTC304
L-T-P: 3-0-0	Credits: 3	Contact Hours: 3Hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 30Hrs	Examination Duration:3 Hrs	

Unit I

Chapter 1: Electrostatic Fields

Introduction, Coulomb's Law and Field Intensity, Electric Fields Due to Continuous Charge Distribution, Electric Flux Density, Gauss's Law – Maxwell's Equation, Application of Gauss's Law, Electric Potential, Relationship between E and V – Maxwell's Equation, An Electric Dipole and Flux Lines, Energy Density in Electrostatic Fields.

Chapter 2: Electric Fields in Material Space

Introduction, Properties of materials, Convection and Conduction Currents, Conductors, Polarization in Dielectrics, Dielectric Constant and strength, Continuity Equation and Relaxation Time, Boundary Conditions.

Chapter 3: Electrostatic Boundary-Value Problems

Introduction, Poisson's and Laplace's Equations, Uniqueness Theorem, General Procedure for Solving Poisson's or Laplace's Equation, Resistance and Capacitance, Method of Images.

Unit II

Chapter 4: Magnetostatic Fields

Introduction, Biot-Savart's Law, Ampere's Circuit Law—Maxwell's Equation, Applications of Ampere's Law, Magnetic Flux Density—Maxwell's Equation, Maxwell's Equations for Static EM Fields, Magnetic Scalar and Vector Potentials, Derivation of Biot-Savart's Law and Ampere's Law.

Chapter 5: Magnetic Forces, Materials and Devices

Introduction, Forces due to Magnetic Fields, Magnetic Torque and Moment, A Magnetic Dipole, Magnetization in Materials, Classification of Magnetic Materials, Magnetic Boundary Conditions, Inductors and Inductances, Magnetic Energy, Magnetic Circuits, Force on Magnetic Materials

Chapter 6: Maxwell's Equations

Introduction, Faraday's Law, Transformer and Motional Electromotive Forces, Displacement Current, Maxwell's Equations in Final Forms, Time-Varying Potentials, Time-Harmonic Fields.

Unit III

Chapter 7: Electromagnetic Wave Propagation

Introduction, Wave Propagation in Lossy Dielectrics, Plane Waves in Lossless Dielectrics, Plane Waves in Free Space, Plane Waves in Good Conductors, Power and the Poynting Vector, Reflection of a Plane Wave at Normal Incidence, Reflection of a Plane Wave at Oblique Incidence.

Text Books

1. Mathew N. O. Sadiku, Elements of Electromagenics, 4th Edition, Oxford University Press, 2007
2. William Hayt, Jr. John A. Buck, Engineering Electromagnetics, 8th edition, TMH, 2012
3. Kraus, John D. Electromagnetics. United Kingdom, McGraw-Hill, 1992.

Back to Semester - V

Program: Electronics Engineering (VLSI Design & Technology)		Semester: V Semester
Course Title: Digital Signal Processing and Architecture		Course Code: 24EVTC305
L-T-P: 3-0-0	Credits: 3	Contact Hours: 4Hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 30Hrs	Examination Duration: 2 Hrs	

Unit I

Chapter No. 1. Introduction to Digital Signal Processing

Brief review of signals and systems: Basic definitions, properties and applications. Discrete Fourier Transforms (DFT), Properties of DFT, overlap-save and overlap-add method. Fast-Fourier-Transform (FFT) algorithms, Radix-2 FFT algorithm for the computation of DFT and IDFT: Decimation-in-time and Decimation-in-frequency algorithms.

Chapter No. 2. Introduction to Filter Design: IIR Filters

Analog filter design, Design of IIR filters from analog filters, impulse invariance method, bilinear transformation, Butterworth and Chebyshev filters

Unit II

Chapter No. 3. Design and Realization of Digital Filters

Design of FIR filters, design of linear phase FIR filters using windowing method- Rectangular, Hamming, Hanning, Bartlet and Kaiser windows. Design of linear phase FIR filters using frequency sampling technique. Structures for FIR systems: direct form I, direct form II, cascade, frequency sampling and lattice structure

Chapter No. 4. Introduction to Programmable Digital Signal Processors

Introduction of DSPs, Classification (2X, 5X, 6X and DaVinci) and applications, Basic Architectural Features, DSP Computational Building Blocks, Bus architecture and memory, Data addressing capabilities, Address generation unit, Programmability and program execution, Speed issues, Features for external interfacing.

Unit III

Chapter No. 5. Programmable Digital Signal Processors

Introduction, Commercial digital Signal-processing Devices, Data Addressing Modes of TMS32OC54xx., Memory Space of TMS32OC54xx Processors, Program Control, Instructions and Programming, On-Chip peripherals, Interrupts of TMS32OC54XX Processors, Pipeline Operation of TMS32OC54xx Processor

Chapter No. 6. VLSI Digital Signal Processing Systems

Introduction, FIR Filters, IIR Filters, design high-speed, low-area, and low-power VLSI systems for a broad range of DSP applications.

Text Books:

1. Proakis&Manolakis, Digital signal processing Principles Algorithms & Applications, 4th edition, PHI, New Delhi, 2007
2. Keshab K. Parhi VLSI Digital Signal Processing Systems: Design and Implementation Wiley Publication, ISBN: 978-0-471-24186-7
3. B Venkatramani and M Bhaskar, Digital Signal Processors: Architectures, Programming and Applications, TMH.

Reference Books:

1. Oppenheim & Schaffer, Discrete Time Signal Processing, 5th edition, PHI, New Delhi, 2000
2. Avatar Singh and S. Srinivasan, “Digital Signal Processing” , Thomson Publishing 2004, Singapore
3. Emmanuel C Ifeachor and B W Jervis, “Digital Signal Processing: A Practical Approach”, Pearson Education, New Delhi.

Back to Semester - V

Program: Electronics Engineering (VLSI Design & Technology)		Semester: V Semester
Course Title: Analog Integrated Circuit Design		Course Code: 24EVTC306
L-T-P: 2-0-1	Credits: 3	Contact Hours: 4Hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 30Hrs	Examination Duration:2 Hrs	

Unit I

Chapter No.1 Basic MOS Device Physics:

General considerations, MOS I/V characteristics, second order effects and MOS device models.

Chapter No.2 Current Mirrors:

Basic current Mirror, Widlar, Cascode and Wilson Current Mirrors.

Chapter No.3 Single Stage Amplifiers:

CS, CG, CD, Cascode and Folded Cascode. Frequency response curves

Unit II

Chapter No. 4: Differential Amplifiers

Differential Amplifier, 5 pack differential Amplifier, CMRR, PSRR

Chapter No. 5 Op-Amp:

Performance parameters, Two stage (7-pack) Op-amp, Slew rate, PSRR, Noise in Op-amps

Chapter No. 6: Compensation Technique

Nyquist stability Criterion, Gain and Phase margins, Compensation of Two stage op-amp and Dominant pole compensation technique.

Unit III

Chapter No. 7: Reference Circuits

Current reference, startup circuits, Bandgap reference circuit, Current mode Bandgap reference.

Chapter No. 8:

Comparators Basic Comparator architecture, non-idealities-offset error, bandwidth consideration, Dynamic comparator.

Text Books:

1. B Razavi 'Design of Analog CMOS Integrated Circuits' First Edition McGraw Hill 2001
2. Phillip. E. Allen, Douglas R. Holberg, "CMOS Analog circuit Design" Oxford University Press, 2002.

Reference Books:

1. Baker, Li, Boyce, "CMOS: Circuit Design, Layout and Simulation", Prentice Hall of India, 2000

Back to Semester - V

Program: Electronics Engineering (VLSI Design & Technology)		Semester: V Semester
Course Title: CMOS VLSI Design Lab		**Course Code: 24EVTP301**
L-T-P: 0-0-1	**Credits: 1**	**Contact Hours: 2Hrs/week**
ISA Marks: 80	**ESA Marks: 20**	**Total Marks: 100**
T eaching Hours: --	**Examination Duration: 2 Hrs**	

List of Experiments:

1. Introduction to Cadence EDA tool.
2. Static and Dynamic Characteristic of CMOS inverter.
3. Layout of CMOS Inverter (DRC, LVS)
4. Static and Dynamic Characteristic of CMOS NAND2 andNOR2.
5. Layout of NAND2, NOR2, XOR2 gates (DRC, LVS).
6. Analysis of Transmission Gate

Structured Enquiry

1. AOI and OAI analysis and layout
2. Design of D-FF

Open Ended

1. Design complex combinational circuits and analyze the performance using Cadence tool.

Reference Books:

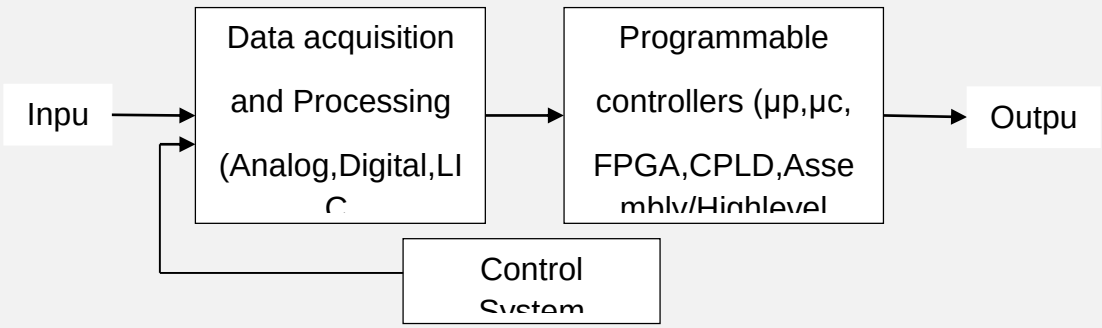
1. John P. Uyemura, -Introduction to VLSI Circuits and Systems, Wiley, 2006.
2. Neil Weste and K. Eshragian, Principles of CMOS VLSI Design: A System Perspective, 2nd edition, Pearson Education (Asia) Ptv. Ltd.,2000.

Back to Semester - V

Program: Electronics Engineering (VLSI Design & Technology)		Semester: V Semester
Course Title: Mini Project		Course Code: 24EVTW301
L-T-P: 0-0-3	Credits: 3	Contact Hours: 6Hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: --	Examination Duration:2 Hrs	

Guide lines for selection of a project:

1. The project needs to encompass the concepts leant in a subject/s studied in the previous four semesters, so that the student will learn to integrate, the knowledge base acquired to provide a solution to the identified need.
2. Project should be able to exhibit sensing, controlling and actuation sections.
3. The mini project essentially will comprise of two components:
   - The hardware design
   - The graphical user interface (GUI) for application and data analysis with report generation.



4. Student can select a project which leads to a product or model or prototype related to following areas (not limited to these areas).
   - Pulse and digital circuits: simulate the working of one or more circuits
   - Signals and systems: simulate the behavior of a system by considering different signals
   - Analog Electronic: simulate working of different devices
   - Control systems: simulate the behavior of a control system
   - Linear Integrated Circuits: simulate working of one or more circuits
   - Micro-controllers: simulate the ALU/control unit of microcontroller
5. Time plan: Effort to do the project should be between 120-150 Hrs per team, which includes self-study of an individual member (80-100 Hrs) and team work (40-50hrs).
6. Learning overhead should be 20-25% of total project development time.

Back to Semester - V

Program: Electronics Engineering (VLSI Design & Technology)		**Semester: V Semester**
Course Title: Arithmetical Thinking and Analytical Reasoning		**Course Code: 23EHSA303**
L-T-P: 0-0-0	**Credits: 0**	**Contact Hours: 1 hrs/week**
ISA Marks: 50	**ESA Marks: 50**	**Total Marks: 100**
Teaching Hours: 16Hrs	**Examination Duration: 3 Hrs**	

Chapter No. 1. Analytical Thinking

Importance of Sense of Analysis for Engineers, Corporate Methodology of Testing Sense of Analysis, Puzzles for practice: Analytical, Mathematical, Classification Puzzles, Teamwork in Problem Solving

Chapter No. 2. Mathematical Thinking I

Problems on Finance: Percentages, Gain and Loss, Interest; Distribution and Efficiency Problems: Averages, Time Work, Permutations Combinations

Chapter No. 3. Mathematical Thinking II

Distribution Problems: Permutations Combinations

Chapter No. 4. Verbal Ability

Comprehension of Passages, Error Detection and Correction Exercises, Common Verbal Ability questions from Corporate Recruitment Tests

Reference Books:

1. George J Summers, “The Great Book of Puzzles & Teasers”, Jaico Publishing House, 1989
2. Shakuntala Devi , “Puzzles to Puzzle You”, Orient Paper Backs, New Delhi, 1976
3. R. S. Aggarwal, “A Modern Approach to Logical Reasoning”, Sultan Chand and Sons, New Delhi, 2018
4. M Tyra, “Magical Book on Quicker Maths”, BSC Publications, 2018
5. Cambridge Advanced Learner’s Dictionary, Cambridge University Press.
6. Kaplan’s GRE guide

Back to Semester - V

Program: Electronics Engineering (VLSI Design & Technology)		Semester: VI Semester
Course Title: Physical Design-Analog		Course Code: 24EVTC307
L-T-P: 1-0-2	Credits: 3	Contact Hours: 5Hrs/week
ISA Marks: 100	ESA Marks: --	Total Marks: 100
Teaching Hours: 14Hrs	Examination Duration:3 Hrs	

Chapter No 1. Standard cell Layout creation

Layout Practice Sessions (DRC/LVS Dirty layout), Understanding verification errors, Error debugging skills, Hands on experience of using layout editor, Quality of the layout, Half DRC rules, Mega module creation.

Chapter No 2. Analog layout

Importance of performance in Analog layout, Importance of floor planning and placement, Attributes need to be taken care during routing stage, Introduction to DRC, LVS, Density and RCX.

Chapter No 3. Matching and Guard rings, Matching

Introduction to mismatch concepts, Causes for mismatch, Types of mis-match, Rules for matching, Activities.

Guard ring: What is guard ring, Usage of guard ring

Chapter No 4. Reliability issues

Introduction to failure mechanism, causes of reliability issues, Process enhancement techniques and Layout considerations to reduce reliability issues

Chapter No 5. Physical design of amplifier and buffer

Applying the studied concepts and doing layout, Prioritising the constraints given, Quality checks, Buddy reviews and implementations, Documentation

Reference Books:

1. Alan Hastings, “The Art of Analog Layout”, 3rd edition, Published by Pearson 2023
2. D. J. Klein, “*CMOS IC Layout: Concepts, Methodologies, and Tools*.”, Hoboken, NJ, USA: Wiley-IEEE Press, 2010.
3. C. Saint and J. Saint, “*IC Layout Basics*.”, New York, NY, USA: McGraw-Hill, 2001.

Back to Semester - VI

Program: Electronics Engineering (VLSI Design & Technology)		Semester: VI Semester
Course Title: VLSI Fabrication Technology		Course Code: 24EVTC308
L-T-P: 2-0-0	Credits: 2	Contact Hours: 2Hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 30Hrs	Examination Duration:3 Hrs	

Unit I

Chapter No. 1: Crystal growth, wafer preparation, epitaxy and oxidation

Electronic Grade Silicon, Czochralski crystal growing, Silicon Shaping, processing considerations, Vapor phase Epitaxy, Molecular Beam Epitaxy, Silicon on Insulators, Epitaxial Evaluation, Growth Mechanism and kinetics, Thin Oxides, Oxidation Techniques and Systems, Oxide properties, Redistribution of Dopants at interface, Oxidation of Poly Silicon, Oxidation inducted Defects.

Unit II

Chapter No. 2: Lithography and relative plasma etching

Optical Lithography, Electron Lithography, X-Ray Lithography, Ion Lithography, Plasma properties, Feature Size control and Anisotropic Etch mechanism, reactive Plasma Etching techniques and Equipment.

Chapter No. 3: Deposition, Diffusion, Ion implementation and Metallization

Deposition process, Poly silicon, plasma assisted Deposition, Models of Diffusion in Solids, Fick's one-dimensional Diffusion Equations – Atomic Diffusion Mechanism – Measurement techniques – Range theory- Implant equipment. Annealing Shallow junctions – High energy implantation – Physical vapor deposition – Patterning.

Unit III

Chapter No. 4: Process simulation and VLSI process integration

Ion implantation – Diffusion and oxidation – Epitaxy – Lithography – Etching and Deposition- NMOS IC Technology – CMOS IC Technology – MOS Memory IC technology - Bipolar IC Technology – IC Fabrication.

Chapter No. 5: Analytical, Assembly Techniques and Packaging of VLSI Devices

Analytical Beams – Beam Specimen interactions - Chemical methods – Package types – packaging design considerations – VLSI assembly technology – Package fabrication technology.

Text Books

1. S.M.Sze, "VLSI Technology", McGraw Hill Second Edition. 1998.
2. James D Plummer, Michael D. Deal, Peter B. Griffin, "Silicon VLSI Technology: Fundamentals Practice and Modeling", Prentice Hall India.2000.
3. Wai Kai Chen, "VLSI Technology" CRC Press, 2003.
4. C.Y. Chang and S.M.Sze (Ed), ULSI Technology, McGraw Hill Companies Inc, 1996.
5. S.K. Gandhi, VLSI Fabrication Principles, John Wiley Inc., New York, 1983.

Back to Semester - VI

Program: Electronics Engineering (VLSI Design & Technology)		Semester: VI Semester
Course Title: System Verilog for Verification		**Course Code: 24EVTC309**
L-T-P: 1-0-2	**Credits: 3**	**Contact Hours: 5Hrs/week**
ISA Marks: 80	**ESA Marks: 20**	**Total Marks: 100**
Teaching Hours: 14Hrs	**Examination Duration:3 Hrs**	

Chapter No. 1. Verification Concepts
Concepts of verification, importance of verification, Stimulus vs Verification, functional verification, test bench generation, functional verification approaches, typical verification flow, stimulus generation, direct testing, Coverage: Code and Functional coverage, coverage plan.

Chapter No. 2. System Verilog – Language Constructs
System Verilog constructs - Data types: two-state data, strings, arrays: queues, dynamic and associative arrays, Structs, enumerated types. Program blocks, module, interfaces, clocking blocks, mod-ports.

Chapter No. 3. System Verilog – Classes & Randomization
SV Classes: Language evolution, Classes and objects, Class Variables and Methods, Class instantiation, Inheritance, and encapsulation, Polymorphism.
Randomization: Directed Vs Random Testing. Randomization: Constraint Driven Randomization.

Chapter No. 4. System Verilog – Assertions & Coverage
Assertions: Introduction to Assertion based verification, Immediate and concurrent assertions. Coverage driven verification: Motivation, Types of coverage, Cover Group, Cover Point, Cross Coverage, Concepts of Binning and event sampling.

Chapter No. 5. Building Testbench
Layered testbench architecture. Introduction to Universal Verification Methodology, Overview of UVM Base Classes and simulation phases in UVM and UVM macros. Unified messaging in UVM, UVM environment structure, Connecting DUT- Virtual Interface

Reference Books:

1. System Verilog LRM
2. Chris Spear, Gregory J Tumbush - SystemVerilog for verification - a guide to learning the testbench language features - Springer, 2012

Tools: Questa Sim, NC Verilog, NC Sim, CVER + GTKWave, VCSMX, Modelsim for Verilog

Back to Semester - VI

Program: Electronics Engineering (VLSI Design & Technology)		Semester: VI Semester
Course Title: GEN AI		Course Code: 24EVTC310
L-T-P: 2-0-1	Credits: 4	Contact Hours: 4 Hrs/week
ISA Marks: 80	ESA Marks: 20	Total Marks: 100
Teaching Hours: 30Hrs	Examination Duration:3 Hrs	

Unit I

Chapter 1: Introduction to Generative AI

Definition, Overview of Generative AI, Importance and applications of Generative AI, Evolution of AI towards generative models, Key milestones and breakthroughs in Generative AI.

Chapter 2: Generative Models I:

Autoencoders (AE) and Variational Autoencoders (VAEs) Architecture: Encoder, Decoder, Latent Space, Training with ELBO (Evidence Lower Bound), Applications and limitations.

Generative Adversarial Networks (GANs): Architecture: Generator and Discriminator, Training process, loss functions, Common issues, Variants: DCGAN, CycleGAN, StyleGAN.

Diffusion Models: Forward process (encoders), reverse process (decoders), score matching, guided diffusion

Chapter 3: Training and Evaluation of Generative AI Models:

Optimization Methods: Gradient Descent, Stochastic Gradient Descent (SGD), Adam Optimizer, Adam (Adaptive Moment Estimation), RMSProp (Root Mean Square Propagation), Adagrad (Adaptive Gradient Algorithm), AdaDelta.

Evaluation Metrics: Inception Score (IS), Frechet Inception Distance (FID), Perplexity, Reconstruction Error, Mode Score, Diversity Metrics, Wasserstein Distance, Earth Mover's Distance (EMD), BLEU Score

Challenges: Mode collapse, stability, and convergence.

Unit II

Chapter 4: Generative Models II: Autoregressive Models

Definition and Principle: Autoregressive Property, Conditional Dependence, Autoregressive Process

Examples of Autoregressive Models: AR Models in Time Series Analysis, Autoregressive Integrated Moving Average (ARIMA)

Autoregressive Models for Generative AI:

PixelCNN - Overview, Architecture, Training, Applications

WaveNet - Overview, Architecture, Training, Applications

Chapter 5: Generative Models II: Transformers

Introduction to Transformers, Origins and evolution from traditional sequence models (like RNNs and LSTMs) to transformers, self-attention mechanism, multi-head attention, position-wise feedforward networks.

Transformer Architecture: breakdown of encoder and decoder stacks, Layer normalization and residual connections, Masked self-attention in the decoder for auto-regressive generation, Pre-training and Fine-tuning.

Transformer-based Autoregressive Models: Overview, Architecture, Training, Applications, BERT (Bidirectional Encoder Representations from Transformers), T5 (Text-to-Text Transfer Transformer)

Chapter 6: Generative Models II: Large Language Models (LLMs)

Introduction to LLMs, Overview of Large Language Models (e.g., GPT-3, GPT-4), Training methodologies and scalability, Integration of LLMs in various generative tasks, Fine-tuning and transfer learning with LLMs, Building and deploying LLM-based applications.
Unit III **Chapter 7: Advanced Topics in Generative AI:** Flow-Based Models, Invertibility, Volume Preservation, Normalizing Flows, Invertible Convolution, Coupling Layers Sparse Attention Mechanisms, Multimodal Generative Models, Meta-Learning and Few-Shot Learning, Continual Learning and Transfer Learning, Privacy-Preserving Generative Models, Quantum Generative Models **Chapter 8: Ethical Considerations and Responsible AI:** Bias and fairness in generative AI models, Privacy concerns and data protection in generative AI applications, Responsible use of generative models in society

Back to Semester - VI

Program: Electronics Engineering (VLSI Design & Technology)		Semester: VI Semester
Course Title: Minor Project		**Course Code: 24EVTW302**
L-T-P: 0-0-6	**Credits: 6**	**Contact Hours: 12Hrs/week**
ISA Marks: 50	**ESA Marks: 50**	**Total Marks: 100**
Teaching Hours: --	**Examination Duration: 3 Hrs**	

Application Areas are,

- Smart City
- Connected Cars
- Home Automation
- Health care
- Smart energy
- Agriculture

Guide lines for selection of a project:

1. The project needs to encompass the concepts leant in a subject/s studied in the previous five semesters, so that the student will learn to integrate, the knowledge base acquired to provide a solution to the defined problem statement of the minor-projects.
2. Student can select a project which leads to a product or model or prototype.
3. Time plan: Effort to do the project should be between 120-150 Hrs per team, which includes self study of an individual member (80-100 Hrs) and team work (40-50hrs).
4. Learning overhead should be 20-25% of total project development time.

Criteria for group formation:

1. 3-4 students in a team.
2. Role of teammates: Team lead and members.

Allocation of Guides and Mentors for the projects:

Every Project batch will be allocated with one faculty.

Details of the project batches:

1. Number of faculty members: 64
2. Number of students: 278

Role of a Guide

The primary responsibility of the guide is to help students to understand the meaning and need of various stages in the implementation of the project. At every stage of the project development, guide should help towards its successful completion as per the predefined standards.

How student should carry out a project:

1. Define the problem
2. Specify the requirements
3. Specify the design in the understandable form (Block Diagram, Flowchart, Algorithm,etc)
4. Analyze the design
5. Select appropriate simulation tool and development board for the design.
6. Implement the design
7. Optimize the design and generate the results with optimized design.
8. Result representation and analysis
9. Prepare a document and presentation.

Report Writing

1. The format for report writing should be downloaded from ftp://10.3.0.3/minorprojects
2. The report needs to be shown to guide and committee for each review.

Back to Semester - VI

Program: Electronics Engineering (VLSI Design & Technology)		**Semester: VI**
Course Title: Industry Readiness & Leadership Skills		**Course Code: 23EHSA304**
L-T-P: 0-0-0	**Credits: 0**	**Contact Hours: 1 hrs/week**
ISA Marks: 25	**ESA Marks: 75**	**Total Marks: 100**
Teaching Hours: 16Hrs	**Examination Duration: 3 Hrs**	

Chapter No. 1. Written Communication

Successful Job Applications, Résumé Writing, Emails, Letters, Business Communication, Essay, and Paragraph Writing for Recruitment Tests

Chapter No. 2. Interview Handling Skills

Understanding Interviewer Psychology, Common Questions in HR Interviews, Grooming, Interview Etiquette

Chapter No. 3. Lateral & Creative Thinking

Lateral Thinking by Edward de Bono, Fractionation and Brain Storming, Mind Maps, Creativity Enhancement through Activities

Chapter No. 4. Team Building & Leadership Skills

Communication in a Team, Leadership Styles, Playing a Team member, Belbin's team roles, Ethics, Effective Leadership Strategies

Reference Books:

1. Diana Booher – E Writing, Laxmi Publications
2. Edward de Bono–Lateral Thinking – A Textbook of Creativity, Penguin UK
3. William Strunk, E B White – The Elements of Style, Pearson
4. John Maxwell – The 17 Essential Qualities of a Team Player, HarperCollins Leadership
5. Robin Ryan – 60 Seconds and You're Hired! – Penguin Books

Back to Semester - VI

Program: Electronics Engineering (VLSI Design & Technology)		Semester: VI Semester
Course Title: Professional Aptitude and Logical reasoning		**Course Code: 23EHSA302**
L-T-P: 3-0-0	**Credits: 3**	**Contact Hours: 3 Hrs/ Week**
ISA Marks: 50	**ESA Marks: 50**	**Total Marks: 100**
Teaching Hours: 40Hrs	**Examination Duration:3 Hrs**	

Unit I

Chapter 1. – Arithmetical Reasoning

Chapter 2. – Analytical Thinking

Chapter 3. – Syllogistic Logic

Unit II

Chapter 1. – Verbal Logic

Chapter 2. – Non-Verbal Logic

Unit III

Chapter 1. - Lateral Thinking

Text Books

1. A Modern Approach to Verbal and Non – Verbal Reasoning – R. S. Aggarwal, Sultan Chand and Sons, New Delhi
2. Quantitative Aptitude – R. S. Aggarwal, Sultan Chand and Sons, New Delhi

Reference Books:

1. Verbal and Non – Verbal Reasoning – Dr. Ravi Chopra, MacMillan India
2. Lateral Thinking – Dr. Edward De Bono, Penguin Books, New Delhi

Back to Semester - VI

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Program: Electronics Engineering (VLSI Design & Technology)		Semester: VI
Course Title: Advanced IC Packaging		Course Code: 24EVTE304
Credits:3	Contact Hours:4 hrs/week	
ESA Marks:--	Total Marks:100	
Examination Duration:3hrs		

Chapter 1: Introduction to Advanced Semiconductor Packaging

- Overview of semiconductor packaging
- Evolution of packaging technologies
- Challenges and trends in advanced packaging

Chapter 2: Packaging Materials and Processes

- Materials used in advanced packaging
- Assembly and packaging processes
- Flip-chip, wafer-level packaging, and 3D packaging
- Thermal and reliability considerations

Chapter 3: System-in-Package (SiP) and Multi-Chip Modules (MCM)

- Introduction to SiP and MCM
- Design considerations for SiP and MCM
- Introduction to SerDes, on-die PHYs and signal integrity

Chapter 4: Advanced Interconnect Technologies

- Microbump and fine-pitch technologies
- Through-Silicon Via (TSV) and 3D interconnects
- High-density interconnects (HDI)

Chapter 5: Layout of Package Substrates (Lecture & Lab)

- Review provided bump-to-ball connectivity data and fill out assigned lab worksheet
- Open single-die package layout database in a commercial package design tool such as APD+ and explore signal routing and power planes, filling out assigned lab worksheet
- Given a bump-to-ball map and substrate layer information, implement substrate layout

Chapter 6: Layout of Silicon Interposers (Lecture & Lab)

- Layout a silicon interposer given a microbump map for an ASIC and C4 ball assignments using a commercial router such as Innovus

Reference Books

1. Rao R Tummala, Fundamentals of Device and Systems Packaging, McGraw Hill, 2020.
2. Glenn R. Blackwell, The Electronics Packaging Handbook, CRC Press, 2017.

3. Bernard S Matisoff, Handbook of Electronics Packaging Design and Engineering, Springer, 2012.
4. Rao R Tummala, Fundamentals of Microsystems Packaging, McGraw Hill, 2001.

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Program: Electronics Engineering (VLSI Design & Technology)		Semester: VI Semester
Course Title: Communication Systems		Course Code: 24EVTE301
L-T-P: 3-0-0	Credits: 3	Contact Hours: 3Hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 40Hrs	Examination Duration:3 Hrs	

Unit I

Chapter 01. Introduction to Analog communication:

Introduction, history of communication, need for modulation, Amplitude modulation, Time-Domain and Frequency domain description, Frequency-Domain description, DSBSC, SSB, VSB, Phase and frequency modulation, Phase and frequency Deviation, Narrow and Wide band frequency modulation. Spectrum and phase diagram of FM Transmission band width of FM waves, Effect of Modulation index on bandwidth, Comparison of all modulation techniques.

Chapter 02. Sampling Process:

Sampling theorem, Quadrature sampling of Band pass signals, Reconstruction of a message from its samples. Time Division Multiplexing (TDM) Signal distortion in Sampling. Pulse Amplitude Modulation (PAM), Pulse Position Modulation (PPM), Pulse Width Modulation (PWM).

Unit II

Chapter 03. Waveform Coding Techniques:

Pulse-Code Modulation, Channel noise and Error Probability, Quantization noise and Signal to noise ratio, Robust Quantization, Differential Pulse code modulation, Delta Modulation, Problems.

Chapter 04. Baseband shaping for data transmission: Discrete PAM signals, Power spectra of discrete PAM signals,Intersymbol Interference, Nyquist'scriterion for distortionless baseband binary transmission, correlative coding, eye pattern, baseband M-ary PAM systems, and adaptive equalization for data transmission, Problems.

Unit III

Chapter 05. Digital Modulation Techniques:

Digital Modulation formats, Coherent binary modulation techniques, Coherent quadrature modulation techniques, Non-coherent binary modulation techniques, Comparison of Binary and Quaternary Modulation techniques, Problems.

Text Books

1. "Communication Systems" by 'Simon Haykin' John Wiley 2003. 5th edition, 2009
2. "Principles of communication Systems", by Taub & Schilling, 2nd edition, TMH.
3. "Digital communications", Simon Haykin, John Wiley, 2006

Reference Books:

1. Communication Systems, by B.P.Lathi ,

2. Ganesh Rao, K N Haribhat, Analog Communication, Sanguine, 2009
3. Communication Systems by Harold. P.E, Stern Samy. A. Mahmond, Pearson Education, 2004.
4. Electronic communication systems, Kennedy and Davis, TMH, Edn. 6, 2012

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Program: Electronics Engineering (VLSI Design & Technology)		Semester: VI Semester
Course Title: Computer Communication Networks		**Course Code: 24EVTE302**
L-T-P: 3-0-0	**Credits: 3**	**Contact Hours: 3 Hrs/week**
ISA Marks: 50	**ESA Marks: 50**	**Total Marks: 100**
Teaching Hours: 40Hrs	**Examination Duration:3 Hrs**	

Unit I

Chapter No.1. Computer Networks and the Internet What is Internet? The Network Edge, the network Core, delay-loss, throughput in packet switched networks. Protocol layers (OSI layers) and their service models, networks under attack

Chapter No. 2. Application Layer Principles of network applications, the web and HTTP, DHCP, electronic mail in the internet, DNS, peer-to-peer applications

Unit II

Chapter No. 3. Transport Layer Introduction and transport-layer services-relationship between transport and network layers - overview of the transport layer in the internet, multiplexing and de multiplexing, connectionless transport: UDP, principles of reliable data transfer, connection-oriented transport TCP, TCP congestion control.

Chapter No. 4. Network layer Introduction, virtual circuit and datagram networks, what's inside router? The Internet protocol (IP): forwarding and addressing in the internet.

Unit III

Chapter No. 5. Network layer:Routing algorithms: Link-State (LS), Distance-Vector (DV), Hierarchical Routing, Routing in the Internet, Intra-AS routing RIP, OSPF, Inter-AS routing BGP, broadcast routing algorithms and multi cast routing

Text Books:

1. Kurose & Ross, Computer Networking A Top-Down Approach, 6th edition, PEARSON, 2013.

Reference Books:

1. Behrouz A. Forouzan, 1. Data Communications and Networking, 4th Edition, Tata McGra, 2006
2. Larry L. Peterson and Bruce S. Davie, Computer Networks A Systems Approach, 4th Edition, Elsevier, 2007

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Program: Electronics Engineering (VLSI Design & Technology)		Semester: VI Semester
Course Title: Embedded Intelligent Systems		Course Code: 24EVTE303
L-T-P: 1-0-2	Credits: 3	Contact Hours: 5Hrs/week
ISA Marks: 80	ESA Marks: 20	Total Marks: 100
Teaching Hours: 14Hrs	Examination Duration:3 Hrs	

1. Basics of embedded systems

Linux Application Programming, System V IPC, Linux Kernel Internals and Architecture, Kernel Core, Linux Device Driver Programming, Interrupts & Timers, Sample shell script, application program, driver source build and execute.

2. Heterogeneous computing

Basics of heterogeneous computing with various hardware architectures designed for specific type of tasks, Advanced heterogeneous computing with a. Introduction to Parallel programming b. GPU programming (OpenCL) c. Open standards for heterogeneous computing (Openvx), Basic OpenCL examples - Coding, compilation and execution.

3. ML Frameworks lab with the target device

Caffe, TensorFlow, TF Lite machine learning frameworks & architecture, Model parsing, feature support and flexibility, supported layers, advantages and disadvantages with each of these frameworks, Android NN architecture overview, Full stack compilation and execution on embedded device.

4. Model Development and Optimization

Significance of on device AI, Quantization, pruning, weight sharing, Distillation, Various pre-trained networks and design considerations to choose a particular pre-trained model, Federated Learning, Flexible Inferencing.

5. Android Anatomy

Android Architecture, Linux Kernel, Binder, HAL Native Libraries, Android Runtime, Dalvik Application framework, Applications, IPC.

Text Books

1. Linux System Programming, by Robert Love, Copyright © 2007 O'Reilly Media
2. Heterogeneous Computing with OpenCL, 2nd Edition by Dana Schaa, Perhaad Mistry, David R. Kaeli, Lee Howes, Benedict Gaster, Publisher: Morgan Kaufmann

Reference Books:

1. Deep Learning, MIT Press book, Goodfellow, Bengio, and Courville's
2. Beginning Android, by Wei-Meng Lee , Publisher: Wrox , O'Reilly Media

Experiment wise plan

Expt./Job No.	Experiment/job Details
1.	Practice programs on Linux Application Programming, system IPC
2.	Implement toolchain, linker, and loaders while building Hello World on the host, then execute on target.
3.	Basic OpenCL examples - Coding, compilation, and execution
4.	High-level language to assembly language translation – optimization and power management.
5.	Implementation of Caffe TensorFlow, TF Lite machine learning frameworks & architecture. Execution of sample programs with various pre-trained models
6.	Full stack compilation and execution on an embedded device. Quantization, pruning, weight sharing, Distillation execution with parameters.
7.	Implement basic programs in the Android framework and implement Android NN architecture.
8.	Push the ML/DL model on an Android device and run the application.
9.	Design an ML/DL model for a given problem targeted at Android devices with different architectures based on provided specifications.

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Program: Electronics Engineering (VLSI Design & Technology)		Semester: VI Semester
Course Title: Automotive Electronics		Course Code: 24EVTE305
L-T-P: 3-0-0	Credits: 3	Contact Hours: 3Hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 40Hrs	Examination Duration:3 Hrs	

Unit I

Chapter No: 1. Introduction to Vehicle Drivelines / Powertrain Systems

Overview of Automotive industry, ECU Design Cycle: Types of model development cycles (V and Agile), Components of ECU, Examples of ECU on Chassis, Infotainment, Body Electronics and cluster. Introduction to power train, manual and automatic transmissions, automotive axles, 4-wheel and 2-wheel drives, Vehicle braking fundamentals, Steering Control, Overview of Hybrid Vehicles.

Chapter No: 2. Automotive Control Systems Design

Derivation of models and design of control strategies for powertrain control modules and integration into automotive platforms. Engine control functions, Fuel control, Electronic systems in Engines, Development of control algorithm for EMS with consideration of vehicle performance. Automotive grade microcontrollers: Architectural attributes relevant to automotive applications, Automotive grade processors ex: Renesas, Quorivva, and Infineon.

Chapter No: 3. Automotive Sensors and Actuators

Sensor characteristics, Sensor response, Sensor error, Redundancy of sensors in ECUs, Avoiding redundancy, Smart Nodes, Examples of sensors: Accelerometer (knock sensors), wheel speed sensors, Engine speed sensor, Vehicle speed sensor, Throttle position sensor, Temperature sensor, Mass air flow (MAF) rate sensor, Exhaust gas oxygen concentration sensor, Throttle plate angular position sensor, Crankshaft angular position/RPM sensor, Manifold Absolute Pressure (MAP) sensor. Actuators: Engine Control Actuators, Solenoid actuator, Exhaust Gas Recirculation Actuator

Unit II

Chapter No:4. Automotive Stability and Safety Systems

Passive/active safety systems and design philosophies. Investigation of stability issues associated with vehicle performance and the use of sensors and control system strategies for stability enhancement. Implementation and application to intelligent cruise control, lane departure warning systems, ABS, Traction Control, active steering systems, vehicle dynamic control systems.

Chapter No:5. Automotive communication protocols

Overview of Automotive communication protocols: CAN, CAN FD, SOME/ IP Protocol, LIN, Flex Ray, MOST

Unit III

Chapter No: 6. Overview of ADAS/AV and Functional safety standards

Advanced Driver Assistance Systems (ADAS), Autonomous vehicle basics, sensing, planning and controls for autonomous driving, connected vehicles.

Functional Safety: Need for safety standard-ISO 26262, safety concept, safety process for product life cycle, safety by design, validation.

Chapter No:7. Diagnostics and Reliability

Discussion of legislated state, federal and international requirements. On-board automotive sensors to monitor vehicle operation, typical diagnostic algorithms. Analytical methods for designing fault-tolerant systems and assessing vehicle reliability, including safety critical systems and 'limp-home' modes. Use of handheld scanners and specialized diagnostic equipment to classify faults. Diagnostic protocols: KWP2000 and UDS.

Text Books:

1. Ribbens, Understanding of Automotive electronics, 8th edition, Elsevier,2017
2. Denton.T, Automobile Electrical and Electronic Systems, 5th edition, Routledge, 2017
3. Denton.T, Advanced automotive fault diagnosis, 4th edition Routledge, 2016

Reference Books:

1. Ronald K Jurgen, Automotive Electronics Handbook, 2nd Edition, McGraw-Hill,1999
2. JamesD Halderman, Automotive electricity and Electronics, 5th edition, Pearson, 2016
3. Allan Bonnick, Automotive Computer Controlled Systems Diagnostic Tools and Techniques, Elsevier Science,2001
4. Nicholas Navet, Automotive Embedded System Handbook ,2009

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Program: Electronics Engineering (VLSI Design & Technology)		Semester: VII Semester
Course Title: CMOS ASIC Design		Course Code: 25EVTC401
L-T-P: 1-0-2	Credits: 3	Contact Hours: 5 Hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 16 Hrs	Examination Duration:3 Hrs	

Chapter No. 1.
Design of combinational and sequential logic gates in CMOS. Layout and characterization of standard cells. Verilog for representing gate level netlists. Sequential circuit timing and static timing analysis. **(2 Hrs)**

Chapter No. 2.
Cell and net delays and cross-talk. Rationale and implementation of scan chains for testing standard-cell based logic circuits. **(2 Hrs)**

Chapter No. 3.
Physical design of standard-cell based CMOS ASICs: scan insertion, placement, clock tree synthesis and routing. **(2 Hrs)**

Chapter No. 4.
Netlist transformations at each step of the physical design process. Net parasitic and parasitic extraction. Use of PLLs for clock generation and deskew. **(2.5 Hrs)**

Chapter No. 5.
Standard data formats for representing technology and design: LEF, Liberary, SDC, DEF and SPEF. Clock gating and power gating for reduction of device power consumption. **(2.5 Hrs)**

Chapter No. 6. Design for reliability: electromigration, wire self heat and ESD checks and fixes. An overview of package design and implementation and system level timing **(2.5 Hrs)**

Case Study : Design of counter (1.5 Hrs)

Reference Books:

1. The Design & Analysis of VLSI Circuits, L. A. Glassey & D. W. Dobbepahl, Addison Wesley Pub Co. 1985.
2. H. Bhatnagar, Advanced ASIC Chip Synthesis Using Synopsys Design Compiler Physical Compiler and PrimeTime, 2nd edition, 2001.
3. Static Timing Analysis for Nanometer Designs A Practical Approach, J. Bhasker • Rakesh Chadha, Springer Science+Business Media, LLC 2009

Tools: Cadence Innovous, Encounter

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Program: Electronics Engineering (VLSI Design & Technology)		Semester: VII
Course Title: Senior Design Project		Course Code: 25EVTW401
L-T-P: 0-0-6	Credits: 6	Contact Hours: 12 hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: --	Examination Duration: 3 Hrs	

- Smart City
- Connected Cars
- Home Automation
- Health care
- Smart energy
- Automation of Agriculture

Guide lines for selection of a project:

- The project needs to encompass the concepts learnt in the previous semesters, so that the student will learn to integrate, the knowledge base acquired to provide a solution to the defined problem statement of the project work.
- Student can select a project which leads to a product or model or prototype.
- Time plan: Effort to do the project should be between 60-70 Hrs per team, which includes self-study of an individual member (80-100 Hrs) and team work (40-50hrs).
- Learning overhead should be 20-25% of total project development time.

Criteria for group formation:

- 3-4 students in a team.
- Role of teammates: Team lead and members.

Allocation of Guides and Mentors for the projects:

Every Project batch will be allocated with one faculty.

Details of the project batches:

- Number of faculty - members: 50
- Number of students:3-4 students in a team.

Role of a Guide

The primary responsibility of the guide is to help students to understand the meaning and need of various stages in the implementation of the project. At every stage of the project development, guide should help towards its successful completion as per the predefined standards.

How student should carry out a project:

- Define the problem.
- Specify the requirements.

- Specify the design in the understandable form (Block Diagram, Flowchart, Algorithm, etc).
- Analyze the design and identify hardware and software components separately.
- Select appropriate simulation tool and development board for the design.
- Implement the design.
- Optimize the design and generate the results.
- Result representation and analysis.
- Prepare a document and presentation.

Report Writing

- The format for report writing should be downloaded from ftp://10.3.0.3/projects
- The report needs to be shown to guide and committee for each review.
-

Evaluation Scheme

- Internal semester assessment (ISA)
- Evaluation is done based on the evaluation rubrics given in Table 1
- Project shall be reviewed and evaluated by the concerned Guide for 50% of the marks.
- Project shall be evaluated by the review committee for 50% of the marks.

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Program: Electronics Engineering (VLSI Design & Technology)		Semester: VII
Course Title: CIPE & EVS		Course Code: 15EHSC402
L-T-P: 2-0-0	Credits: Audit	Contact Hours: 2 hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 30Hrs	Examination Duration: 3 Hrs	

Unit I

Chapter No. 1 Features of Indian Constitution

Features of Indian Constitution, Preamble to the constitution of India, Fundamental rights under Part III – details of Exercise of rights, Limitations & Important cases. Berubari Union and Exchange of Enclaves, KesavanandBharati vs. UOI, Maneka Gandhi vs. UOI, Air India Ltd. vs. NargeesMeerza, T.M.A. Pai Foundation v. St. of Karnataka, M.C. Mehta vs. UOI etc.,

Chapter No. 2 Relevance of Directive principles of State Policy

Relevance of Directive principles of State Policy under Part IV, Fundamental duties & their significance. SarlaMudgal v. UOI

Chapter No. 3 Union

Union – President, Vice President, Union Council of Ministers, Prime Minister, Parliament & the Supreme Court of India.

Chapter No.4 State

State – Governors, State Council of Ministers, Chief Minister, State Legislature and Judiciary.

Chapter No. 5 Constitutional Provisions for Scheduled Castes & Tribes

Constitutional Provisions for Scheduled Castes & Tribes, Women &Children & Backward classes, Emergency Provisions.

Chapter No. 6 Electoral process

Electoral process, Amendment procedure, 42nd, 44th and 86th Constitutional amendments.

Unit II

Chapter No. 7 Scope & Aims of Engineering Ethics

Scope & Aims of Engineering Ethics: Meaning and purpose of Engineering Ethics, Responsibility of Engineers, Impediments to responsibility, Honesty, Integrity and reliability, risks, safety & liability in engineering. Bhopal Gas Tragedy, Titanic case.

Chapter No. 8 Intellectual Property Rights

Intellectual Property Rights (IPRs)- Patents, Copyright and Designs

Chapter No. 9 Ethical perspectives of professional bodies

Ethical perspectives of professional bodies- IEEE, ASME, NSPE and ABET, ASCE etc.

Unit III

Chapter No. 10 Effects of human activities on environment

Effects of human activities on environment - Agriculture, Housing, Industry, Mining, and Transportation activities, Environmental Impact Assessment, Sustainability and Sustainable Development.

Chapter No. 11 Environmental Protection

Environmental Protection – Constitutional Provisions and Environmental Laws in India.

Text Book (List of books as mentioned in the approved syllabus)

1. Dr. J. N. Pandey, “Constitutional Law of India”, Central Law Agency, 2005
2. Dr. M.K. Bhandari, “Law relating to Intellectual Property Rights”, Central Law Publicaitons, Allahabad, 2010.
3. Charles E. Harris and others, “Engineering Ethics: Concepts and Cases”, Thomson Wadsworth, 2003

References

1. Durga Das Basu, “Introduction to the Constitution of India”, Prentice-hall EEE, 2001
2. Mike Martin and Ronald Schinzinger, “Ethics in Engineering”, Tata McGraw-Hill Publications.

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Program: Electronics Engineering (VLSI Design & Technology)		Semester: VII Semester
Course Title: Design for Testability		**Course Code: 25EVTE402**
L-T-P: 1-0-2	**Credits: 3**	**Contact Hours: 5 Hrs/week**
ISA Marks: 67	**ESA Marks: 33**	**Total Marks: 100**
Teaching Hours: 16 Hrs	**Examination Duration:2 Hrs**	

Chapter No. 1. Introduction to Design for Testability

- Overview of the importance of design for testability in modern electronic systems.
- Historical context and evolution of testability strategies.
- Introduction to key concepts: fault models, testing methodologies, and industry standards **(3 Hrs)**

Chapter No. 2. Built-in Self-Test (BIST) Techniques

- Principles and implementation of built-in self-test techniques.
- Advantages and limitations of BIST in electronic circuit testing.
- Lab sessions: Simulations and exercises focusing on BIST. **(3 Hrs)**

Chapter No. 3. Scan Chains and Serial Testing

- Concept of scan chains and their role in serial testing.
- Implementation and optimization of scan chains for improved testability.
- Lab sessions: Hands-on exercises with scan chain design and testing **(2 Hrs)**

Chapter No. 4. Fault Modeling and Simulation

- Development of fault models for electronic circuits.
- Utilization of simulation tools to predict and analyze potential faults in a design.

and deskew. **(2 Hrs)**

Chapter No. 5. Design for Testability Strategies

- Exploration of various design for testability strategies.
- Case studies: Analyzing successful implementations of design for testability.**(1.5 Hrs)**

Chapter No. 6. Industry Standards in Testability

- Overview of industry standards related to testability.
- Compliance and certification requirements for testable designs. **(1.5 Hrs)**

Reference Books:

1. Tripathi, Suman. Advanced VLSI Design and Testability Issues. CRC Press, 2020.
2. Wang, Laung-Terng. VLSI Test Principles and Architectures. Morgan Kaufmann, 2006.
3. Huhn, Sebastian. Design for Testability, Debug and Reliability. Springer Nature, 2021.

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Program: Electronics Engineering (VLSI Design & Technology)		Semester: VII
Course Title: EMC & Signal Integrity		Course Code: 25EVTE416
L-T-P: 1-0-2	Credits: 3	Contact Hours: 5 hrs/week
ISA Marks: 67	ESA Marks: 33	Total Marks: 100
Teaching Hours: 20 Hrs	Examination Duration: 2 Hrs	

Unit I

Chapter No. 1. Introduction to EMC and Signal Integrity

- Overview of Electromagnetic Compatibility (EMC) and Signal Integrity
- Importance of EMC in electronic systems and its impact on signal integrity **(3 Hrs)**

Chapter No. 2. EMC Standards and Regulations

- Study of international EMC standards and regulatory requirements
- Case studies on the consequences of non-compliance **(4 Hrs)**

Unit II

Chapter No. 3. Signal Integrity Fundamentals

- Fundamentals of signal integrity in high-speed digital and mixed-signal designs
- Analysis of transmission line effects, reflections, and signal degradation **(3 Hrs)**

Chapter No. 4. PCB Layout Considerations

- PCB layout techniques for EMC and signal integrity
- High-speed routing guidelines, power distribution, and grounding strategies **(4 Hrs)**

Unit III

Chapter No. 5. EMI Mitigation Techniques

- Strategies for minimizing electromagnetic interference (EMI)
- Filtering, shielding, and grounding techniques for EMI mitigation **(3 Hrs)**

Chapter No. 6. Simulation Tools for Signal Integrity

- Introduction to simulation tools for signal integrity analysis
- Hands-on exercises using simulation software to predict and optimize signal integrity. **(3 Hrs)**

References:

1. Bogatin, Eric. Signal and Power Integrity - Simplified. Prentice Hall, 2017.
2. Montrose, Mark. EMC and the Printed Circuit Board. John Wiley & Sons, 2004.
3. Christopoulos, Christos. Principles and Techniques of Electromagnetic Compatibility. CRC Press, 2018.
4. Russ, Samuel. Signal Integrity. Springer Nature, 2022.

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Program: Electronics Engineering (VLSI Design & Technology)		Semester: VII Semester
Course Title: Hardware-Software Co-design		**Course Code: 25EVTE407**
L-T-P: 3-0-0	**Credits: 3**	**Contact Hours: 3Hrs/week**
ISA Marks: 50	**ESA Marks: 50**	**Total Marks: 100**
Teaching Hours: 40Hrs	**Examination Duration:3 Hrs**	

Unit I

Introduction to Hardware Software Codesign Models taxonomy, State-Oriented & Activity Oriented Models, Structure & Data–Oriented Models Architectural Models Introduction to Linux and Ptomley Introduction to Specification Languages Profiling, Benchmarks and SystemC.

Unit II

Polis framework System Partitioning issues Introduction to Low power issues Dynamic Power Management (DVS and DPM). YDS algorithm. Hardware / Software Co-Synthesis Software Power Management. Cache Power Minimization. Design Quality Estimation AMBA Bus Design & LEON3 platform.

Unit III

Compilation Techniques, Device drivers, Case Study

Text Books:

1. Daniel D Gajski, Frank Vahid, Sanjay Narayan, Jie Gong, Specification and Design of Embedded Systems, Prentice Hall, 1994.
2. (T2) Peter Marwedel, Embedded System Design, Kluwer Academic Publishers, 2003, ISBN: 1402076908

Reference Books:

1. G. DeMicheli, R. Ernst and W. Wolf, Readings in Hw/Sw Co-design, M. Kaufmann, 2002.

2. Ahmed A. Jerraya and Jean Mermet eds.: System Level Synthesis, Kluwer 1999.

3. Hardware/Software Codesign. G. DeMicheli and M. Sami (eds.), NATO ASI Series E, Vol. 310, 1996.

4. Sanjaya Kumar, James H. Aylor, Barry W. Johnson, and Wm. A. Wulf. The Codesign of Embedded Systems. Kluwer, 1995

5. IEEE and ACM Transactions. 6. Jorgen Staunstrup, Wayne Wolf, Hardware / Software Co-Design: Principles and Practice, Kluwer Academic, 1997 7. Black David C. Systemc : From The Ground Up

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Program: Electronics Engineering (VLSI Design & Technology)		**Semester: VII Semester**
Course Title: Analog and Mixed mode VLSI Circuits		**Course Code: 25EVTE413**
L-T-P:3-0-0	**Credits:3**	**Contact Hours:3hrs/week**
ISA Marks:50	**ESA Marks:50**	**Total Marks:100**
Teaching Hours:40hrs	**Examination Duration:3hrs**	

Unit I

Chapter 01: Data Converter Fundamentals: Analog Versus Discrete Time Signals, Converting Analog Signals to Digital Signals, Sample-and-Hold (S/H) Characteristics, Digital-to-Analog Converter (DAC) Specifications, Specifications

Chapter 02: Data Converter Architectures: Resistor String, R-2R Ladder Networks, Charge-Scaling DACs, Cyclic DAC, Pipeline DAC.

Unit II

Chapter 03: ADC Architectures: Flash ADC, The Two-Step Flash ADC, The Pipeline ADC, Integrating ADCs, The Successive Approximation ADC, The Oversampling ADC

Unit III

Chapter 06: PLL-operating principles, Phase detector and VCO; Phase frequency Detector, Charge pump models, stability issues, Jitter in PLL.

Text Books

1. Phillip. E. Allen, Douglas R. Holberg, "CMOS Analog circuit Design" Oxford University Press, 2002.
2. Baker, Li, Boyce, "CMOS: Circuit Design, Layout and Simulation", Prentice Hall of India, 2000

Reference Books

1. N. Weste and K. Eshranghian, Principles of CMOS VLSI Design, Addison Wesley. 1985.
2. J. Rabaey, Digital Integrated Circuits: A Design Perspective, Prentice Hall India, 1997
3. C. Mead and L. Conway, Introduction to VLSI Systems, Addison Wesley, 1979.
4. B Razavi 'Design of Analog CMOS Integrated Circuits' First Edition McGraw Hill 2001

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Program: Electronics Engineering (VLSI Design & Technology)		Semester: VII Semester
Course Title: Memory Design and Testing		**Course Code: 25EVTE401**
L-T-P: 3-0-0	**Credits: 3**	**Contact Hours: 3Hrs/week**
ISA Marks: 50	**ESA Marks: 50**	**Total Marks: 100**
Teaching Hours: 40Hrs	**Examination Duration:3 Hrs**	

Unit I

Volatile memories

SRAM – SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, SOI technology, Advanced SRAM architectures and technologies, soft error failure in SRAM, Application specific SRAMs, DRAM – DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failure in DRAM, Advanced DRAM design and architecture, Application specific DRAMs

Non-volatile memories

Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture.

Unit II

Memory Testing and Patterns

General Fault Modeling – Read Disturb Fault Model – Precharge Faults – False Write Through Data Retention Faults – Decoder Faults. Megabit DRAM Testing Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing Application Specific Memory Testing – Zero/one Pattern – Exhaustive Test Patterns – Walking, Matching and Galloping – Pseudo Random Pattern – CAM pattern

Design For Test and BIST

RAM Built-In Self – Test (BIST)-Weak Write Test mode – Bit Line Contact Resistance – PFET Test – Shadow Write and Shadow Read.

Reliability and Radiation Effects

General Reliability Issues-RAM Failure Modes and Mechanism-Nonvolatile Memory Reliability-Design for Reliability Radiation Effects-Single Event Phenomenon (SEP)- Radiation Hardening Techniques Radiation Hardening Process and Design Issues-Radiation Hardened Memory Characteristics

Unit III

Advanced Memory Technologies 08 hours

High-Density Memory Packaging Technologies Ferroelectric Random Access Memories (FRAMs)-Analog Memories-Magneto-resistive Random Access Memories (MRAMs)- Experimental Memory Devices Memory Hybrids and MCMs (2D)- Memory Stacks and MCMs (3D)-Memory MCM Testing and Reliability

Text Books:

1. Sharma, A. K., Advanced Semiconductor Memories: Architecture, Design and Applications, John Wiley (2002).

2. M. Bushnell, V. Agrawal, “Essentials of Electronic Testing for Digital, Memory & Mixed-Signal VLSI Circuits”, Springer, 1st edition, 2nd printing 2005.

3. Brent Keeth, R. Jacob Baker, Brian Johnson, Feng Lin, “DRAM Circuit Design: Fundamental and High-Speed Topics”, 2E, Wiley, IEEE Press December 2007.

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Program: Electronics Engineering (VLSI Design & Technology)		Semester: VII Semester
Course Title: System on Chip Design		Course Code: 25EVTE404
L-T-P: 3-0-0	Credits: 3	Contact Hours: 3Hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 40Hrs	Examination Duration:3 Hrs	

Unit I

Chapter No. 1: Introduction

Introduction: Driving Forces for SoC - Components of SoC - Design flow of SoC Hardware/Software nature of SoC - Design Trade-offs - SoC Applications

Chapter No. 2: System Level Design

System-level Design: Processor selection-Concepts in Processor Architecture: Instruction set architecture (ISA), elements in Instruction Handing-Robust processors: Vector processor, VLIW, Superscalar, CISC, RISC—Processor evolution: Soft and Firm processors, Custom Designed processors- on-chip memory.

Unit II

Chapter No. 3: On-chip bus and IP based design

Interconnection: On-chip Buses: basic architecture, topologies, arbitration and protocols, Bus standards: AMBA, Core Connect, Wishbone, Avalon - Network-on chip: Architecture topologies-switching strategies - routing algorithms flow control, Quality-of-Service- Reconfigurability in communication architectures. IP based system design: Introduction to IP Based design, Types of IP, IP across design hierarchy, IP life cycle, Creating and using IP - Technical concerns on IP reuse – IP integration - IP evaluation on FPGA prototypes.

Chapter No. 4: SoC Implementation

SOC implementation: Study of processor IP, Memory IP, wrapper Design - Real-time operating system (RTOS), Peripheral interface and components, High-density FPGAs - EDA tools used for SOC design.

Unit III

Chapter 5: SoC Testing

SOC testing: Manufacturing test of SoC: Core layer, system layer, application layer-P1500 Wrapper Standardization-SoC Test Automation (STAT).

Text Books:

1. Michael J.Flynn, Wayne Luk, “Computer system Design: Systemon-Chip”, Wiley-India, 2012.

2. Sudeep Pasricha, Nikil Dutt, “On Chip Communication Architectures: System on Chip Interconnect”, Morgan Kaufmann Publishers, 2008.

3. W.H.Wolf, “Computers as Components: Principles of Embedded Computing System Design”, Elsevier, 2008.

Reference Books:

1. Patrick Schaumont “A Practical Introduction to Hardware/Software Co-design”, 2nd Edition, Springer, 2012.

2. Lin, Y-L.S. (ed.), “Essential issues in SOC design: designing complex systems-on-chip. Springer,

2006.
3. Wayne Wolf, “Modern VLSI Design: IP Based Design”, Prentice-Hall India, Fourth edition, 2009.

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Program: Electronics Engineering (VLSI Design & Technology)		Semester: VII Semester
Course Title: Design and Analysis of Algorithm		Course Code: 25EVTE405
L-T-P: 3-0-0	Credits: 3	Contact Hours: 3Hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 40Hrs	Examination Duration:3 Hrs	

Unit I

INTRODUCTION: Algorithm, pseudo code for expressing algorithms, performance analysis-space complexity, time complexity, asymptotic notation- big (O) notation, omega notation, theta notation and little (o) notation, recurrences, probabilistic analysis, disjoint set operations, union and find algorithms.

DIVIDE AND CONQUER: General method, applications-analysis of binary search, quick sort, merge sort, AND OR Graphs. GREEDY METHOD: General method, Applications-job sequencing with deadlines, Fractional knapsack problem, minimum cost spanning trees, Single source shortest path problem.

Unit II

GRAPHS (Algorithm and Analysis): Breadth first search and traversal, Depth first search and traversal, Spanning trees, connected components and bi-connected components, Articulation points. DYNAMIC PROGRAMMING: General method, applications - optimal binary search trees, 0/1 knapsack problem, All pairs shortest path problem, Travelling sales person problem, Reliability design.

BACKTRACKING: General method, Applications- n-queen problem, Sum of subsets problem, Graph coloring and Hamiltonian cycles. BRANCH AND BOUND: General method, applications - travelling sales person problem, 0/1 knapsack problem- LC branch and bound solution, FIFO branch and bound solution.

Unit III

NP-HARD AND NP-COMPLETE PROBLEMS:

Basic concepts, non-deterministic algorithms, NP-hard and NP-complete classes, Cook‘s theorem.

Text Books:

1. Ellis Horowitz, Satraj Sahni, Rajasekharam (2007), Fundamentals of Computer Algorithms, 2nd edition, University Press, New Delhi.

Reference Books:

1. R. C. T. Lee, S. S. Tseng, R.C. Chang and T. Tsai (2006), Introduction to Design and Analysis of Algorithms A strategic approach, McGraw Hill, India.

2. Allen Weiss (2009), Data structures and Algorithm Analysis in C++, 2nd edition, Pearson education, New Delhi.

3. Aho, Ullman, Hopcroft (2009), Design and Analysis of algorithms, 2nd edition, Pearson education, New Delhi

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Program: Electronics Engineering (VLSI Design & Technology)		Semester: VII Semester
Course Title: RF Circuit Design		**Course Code: 25EVTE406**
L-T-P: 3-0-0	**Credits: 3**	**Contact Hours: 3Hrs/week**
ISA Marks: 50	**ESA Marks: 50**	**Total Marks: 100**
Teaching Hours: 40Hrs	**Examination Duration:3 Hrs**	

Unit I

Introduction to RF Design and Wireless Technology: Design and Applications, Complexity and Choice of Technology. Basic concepts in RF design: Nonlinearly and Time Variance, Inter symbol interference, random processes and noise. Sensitivity and dynamic range, conversion of gains and distortion .

RF Modulation: Analog and digital modulation of RF circuits, Comparison of various techniques for power efficiency, Coherent and non-coherent detection, Mobile RF communication and basics of Multiple Access techniques. Receiver and Transmitter architectures, Direct conversion and two-step transmitters.

Unit II

RF Testing: RF testing for heterodyne, Homodyne, Image reject, Direct IF and sub sampled receivers. **BJT and MOSFET behavior at RF Frequencies:** BJT and MOSFET behavior at RF frequencies, modeling of the transistors and SPICE model, Noise performance and limitations of devices, integrated parasitic elements at high frequencies and their monolithic implementation**.**

Unit III

RF Circuits Design: Overview of RF Filter design, Active RF components & modeling, Matching and Biasing Networks. Basic blocks in RF systems and their VLSI implementation, Low noise Amplifier design in various technologies, Design of Mixers at GHz frequency range, Various mixersworking and implementation. Oscillators- Basic topologies VCO and definition of phase noise, Noise power and trade off. Radio frequency Synthesizers- PLLS, Various RF synthesizer architectures and frequency dividers, Design issues in integrated RF filters.

Text Books:

1. . B. Razavi, “RF Microelectronics” PHI 1998

2. R. Jacob Baker, H.W. Li, D.E. Boyce “CMOS Circuit Design, layout and Simulation”, PHI

Reference Books:

1. Thomas H. Lee “Design of CMOS RF Integrated Circuits” Cambridge University press 1998.

2. Y.P. Tsividis, “Mixed Analog and Digital Devices and Technology”, TMH 1996

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Program: Electronics Engineering (VLSI Design & Technology)		Semester: VII Semester
Course Title: Computer-Aided VLSI Design		**Course Code: 25EVTE408**
L-T-P: 3-0-0	**Credits: 3**	**Contact Hours: 3Hrs/week**
ISA Marks: 50	**ESA Marks: 50**	**Total Marks: 100**
Teaching Hours: 40Hrs	**Examination Duration:3 Hrs**	

Unit I

Chapter No. 1: Introduction

Introduction to VLSI design methodologies and supporting CAD environment. Schematic editors: Parsing: Reading files, describing data formats, Graphics & Plotting Layout. Layout Editor: Turning plotter into an editor. Layout language: Parameterized cells, PLA generators.

Chapter No. 2: Silicon Compiler

Introduction to Silicon compiler, Data path, Compiler, Placement & routing, Floor planning.

Unit II

Chapter No. 3: Layout Analysis and Simulations

Layout Analysis: Design rules, Object based DRC, Edge based layout operations. Module generators. Simulation: Types of simulation, Behavioral simulator, logic simulator, functional simulator & Circuit simulator. Simulation Algorithms: Compiled code and Event-driven. Optimization Algorithms: Greedy methods, simulated annealing, genetic algorithm and neural models.

Chapter No. 4: Testing ICs

Testing ICs: Fault simulation, Aids for test generation and testing. Computational complexity issues: Big Oh and big omega terms.

Unit III

Chapter 5: Recent Topics in CAD-VLSI

Recent topics in CAD-VLSI: Array compilers, hardware software co-design, high-level synthesis tools and VHDL modeling.

Text Books:

1. Stephen Trimberger," Introduction to CAD for VLSI", Kluwer Academic publisher, 2002
2. Naveed Shervani, "Algorithms for VLSI physical design Automation", Kluwer Academic Publisher, Second edition.

Reference Books:

1. Gaynor E. Taylor, G. Russell, "Algorithmic and Knowledge Based CAD for VLSI", Peter peregrinus ltd. London.

2. Gerez, "Algorithms VLSI Design Automation", John Wiley & Sons.

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Program: Electronics Engineering (VLSI Design & Technology)		Semester: VII Semester
Course Title: Power Management IC (Swayam)		Course Code: 25EVTE409
L-T-P: 0-0-3	Credits: 3	Contact Hours: 6Hrs/week
ISA Marks: 100	ESA Marks: 00	Total Marks: 100
Teaching Hours: 40Hrs	Examination Duration:3 Hrs	

Unit I

Chapter 1. Basic Concepts of Power Management

Introduction to Power Management; Performance Parameters. Sub-1-volt Bandgap Reference;

Chapter 2. Linear Regulators

Introduction to Linear Regulator, Applications of Linear Regulator; : Miller Compensation, R.H.P. zero due to Miller Compensation, Intuitive Methods of Determining Poles and Zeros after Miller Compensation, Static Offset Correction, Dynamic Offset Cancellation; Digital LDO, Avoidance of Limit Cycle Oscillations in a Digital LDO, : Hard Switching Loss, Magnetic Loss, Relative Significance of Losses as a Function of the Load Current

Unit II

Chapter 3. Buck Converters

Compensating a Voltage-Mode-Controlled Buck Converter; Designing Type-I (Integral), Type-II (PI) and Type-III (PID) Compensators; Designing Type-III Compensator using Gm-C Architecture and Design Example, Designing the Gate-Driver (Gate Buffer and Non-Overlap Clock Generator) Non-Linear Control Techniques for DC-DC Converters; Hysteretic Control

Unit III

Chapter 4: PMIC Layout

Selecting the Process Node for a PMIC, Board-Level Layout Guidelines, EMI Considerations Introduction to Advanced Topics in Power Management

Text Books:

1. Switch-Mode Power Supplies: SPICE Simulations and Practical Designs by Christophe P. Basso, McGraw-Hill Professional, 2008.
2. Fundamentals of Power Electronics, 2nd edition by Robert W. Erickson, Dragan Maksimovic, Springer, 2001.
3. Power Management Techniques for Integrated Circuit Design By Ke-Horng Chen, Wiley-Blackwell, 2016.
4. Design of Analog CMOS Integrated Circuits by Behzad Razavi, McGraw-Hill, 2017.

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Program: Electronics Engineering (VLSI Design & Technology)		Semester: VII Semester
Course Title: Testing & Characterization		Course Code: 25EVTE410
L-T-P:2-0-1	Credits:3	Contact Hours:4hrs/week
ISA Marks:67	ESA Marks:33	Total Marks:100
Teaching Hours:40hrs	Examination Duration:2hrs	

Unit I

Introduction:

Scope of testing and verification in VLSI design process; Issues in test and verification of complex chips; embedded cores and SOCs.

Fundamentals of VLSI testing

Fault models. Automatic test pattern generation, Design for testability, Scan design, Test interface and boundary scan.

Testing

Unit II

System testing and test for SOCs, IDDQ testing, Delay fault testing, BIST for testing of logic and memories, Test automation.

Design verification techniques

Design verification techniques based on simulation, analytical and formal approaches, Functional verification

Unit III

Verification techniques

Timing verification, Formal verification, Basics of equivalence checking and model checking, Hardware emulation.

Text Book:

1. M. Abramovici, M. A. Breuer and A. D. Friedman, "Digital Systems Testing and Testable Design", IEEE Press, 1990.(Available as JAICO Publication)
2. M. Bushnell and V. D. Agarwal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2000.
3. T .Kropf, "Introduction to Formal Hardware Verification", Springer Verlag, 2000.

Reference Books:

1. P. Rashinkar, Paterson and L. Singh, "System-on-a-Chip Verification-Methodology and Techniques", Kluwer Academic Publishers, 2001.
2. M. Abramovici, M. A. Breuer, A. D. Friedman, “Digital Systems Testing and Testable Design” Piscataway, New Jersey: IEEE Press, 1994
3. J.DiGiacomo, editor, “VLSI Handbook”, McGraw-Hill, 1989.
4. Samiha Mourad and Yervant Zorian, “Principles of Testing Electronic Systems”, Wiley (2000).

5. D. K. Pradhan (Editor). Fault-Tolerant Computing: Theory and Techniques, Prentice Hall, NJ, 1986.
6. Miczo. Digital Logic Testing and Simulation, John Wiley & Sons, 1987.
7. Barry Johnson. Design and Analysis of Fault-Tolerant Digital Systems, Addison Wesley, 1989.

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Program: Electronics Engineering (VLSI Design & Technology)		**Semester: VII Semester**
Course Title: Phase-locked loops(Swayam)		**Course Code:25EVTE411**
L-T-P: 0-0-3	**Credits:3**	**Contact Hours:6 hrs/week**
ISA Marks:100	**ESA Marks:**	**Total Marks:100**
Teaching Hours:42Hrs	**Examination Duration:3Hrs**	

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Program: Electronics Engineering (VLSI Design & Technology)		Semester: VII Semester
Course Title: Advanced Computer Architecture		**Course Code: 25EVTE412**
L-T-P: 3-0-0	**Credits: 3**	**Contact Hours: 3Hrs/week**
ISA Marks: 50	**ESA Marks: 50**	**Total Marks: 100**
Teaching Hours: 40Hrs	**Examination Duration:3 Hrs**	

Unit I

PARALLEL COMPUTER MODELS

Evolution of Computer architecture, system attributes to performance, Multi processors and multi computers, Multi-vector and SIMD computers, PRAM and VLSI models-Parallelism in Programming, conditions for Parallelism-Program Partitioning and Scheduling-program flow Mechanisms-Speed up performance laws-Amdahl's law, Gustafson's law-Memory bounded speedup Model.

MEMORY SYSTEMS AND BUSES

Memory hierarchy-cache and shared memory concepts-Cache memory organization-cache addressing models, Aliasing problem in cache, cache memory mapping techniques-Shared memory organization-Interleaved memory organization, Lower order interleaving, Higher order interleaving. Back plane bus systems-Bus addressing, arbitration and transaction.

Unit II

ADVANCED PROCESSORS

Instruction set architectures-CISC and RISC scalar processors-Super scalar processors-VLIW architecture- Multivector and SIMD computers-Vector processing principles-Cray Y-MP 816 system-Inter processor communication.

MULTI PROCESSOR AND MULTI COMPUTERS

Multiprocessor system interconnects- Cross bar switch, Multiport memory-Hot spot problem, Message passing mechanisms-Pipelined processors-Linear pipeline, on linear pipelineInstruction pipeline design-Arithmetic pipeline design.

Unit III

DATA FLOW COMPUTERS AND VLSI COMPUTATIONS

Data flow computer architectures-Static, Dynamic-VLSI Computing Structures-Systolic array architecture, mapping algorithms into systolic arrays, Reconfigurable processor array-VLSI matrix arithmetic processors-VLSI arithmetic models, partitioned matrix algorithms, matrix arithmetic pipelines

Text Books:

1. Kai Hwang, Advanced Computer architecture Parallelism , scalablity ,Programmablity , Mc Graw Hill,N.Y, 2003
2. Kai Hwang and F.A.Briggs, Computer architecture and parallel processor' Mc Graw Hill, N.Y, 1999

References:

1. David A. Pearson and John L. Hennessey, —Computer organization and design Elsevier, Fifth edition, 2014.
2. www.sci.tamucc.edu/~sking/Courses/COSC5351/syllabus.php

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Program: Electronics Engineering (VLSI Design & Technology)		Semester: VII Semester
Course Title: Low Power VLSI Circuits		**Course Code: 25EVTE417**
L-T-P: 3-0-0	**Credits: 3**	**Contact Hours: 3Hrs/week**
ISA Marks: 50	**ESA Marks: 50**	**Total Marks: 100**
Teaching Hours: 40Hrs	**Examination Duration:3 Hrs**	

Unit I

Chapter 1: Introduction to low power VLSI design: Need for Low Power VLSI Chips, sources of power dissipation. Device and Technology impact on Low Power, dynamic power dissipation in CMOS. Power Estimation.

Chapter 2: Power analysis: Simulation Power Analysis, Spice circuit's simulator, gate level logic simulator, Probabilistic power analysis.

Chapter 3: A new CMOS driver model for transient analysis and power dissipation analysis, low power design of off-chip drivers and transmission lines: a branch and bound approach

Unit II

Chapter 4: Different levels of power optimization

Low Power Design; circuit Level, logic Level, Low Power Architecture.

Chapter 5: Floor plan design with low power considerations, optimal drivers of high-speed low power ICs, retiming sequential circuits for low power

Chapter 6: Clock Distribution: Low Power Clock distribution, single driver versus distributed buffers. Power management: Power & performance management, switching activity reduction, parallel architecture.

Unit III

Chapter 7: Algorithmic level methodologies for power reduction: Algorithm and architectural level methodologies- algorithmic level analysis & optimization, architecture level estimation and synthesis, Current trends.

Text Books

1. Gary K. Yeap, "Practical Low Power Digital VLSI Design", KAP, 2002.
2. Rabaey, Pedram, "Low power design methodologies" Kluwer Academic, 1997.

Reference Books:

1. A. Chandrakasan and R. Brodersen, "Low Power CMOS Design".
2. Sung - Mo Kang & Yosuf Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design", TMH, 2003 (Third Edition).
3. Laung-Terng Wang, Charles E. Stroud, Nur A. Touba, "System-on-chip Test Architectures", 2008.
4. Kaushik Roy, Sharat Prasad, "Low-Power CMOS VLSI Circuit Design" Wiley, 2000.

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Program: Electronics Engineering (VLSI Design & Technology)		**Semester: VII Semester**
Course Title: VLSI Interconnects (Swayam)		**Course Code:25EVTE418**
L-T-P: 0-0-3	**Credits:3**	**Contact Hours:6 hrs/week**
ISA Marks:100	**ESA Marks:**	**Total Marks:100**
Teaching Hours:42Hrs	**Examination Duration:3Hrs**	

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Program: Electronics Engineering (VLSI Design & Technology)		Semester: VIII
Course Title: OOPS using C++		Course Code: 25EVTE414
L-T-P: 2-0-1	Credits:3	Contact Hours: 4 hrs/week
ISA Marks:67	ESA Marks:33	Total Marks:100
Teaching Hours:16Hrs	Examination Duration:2Hrs	

UNIT I

Chapter 1: Fundamental concepts of object oriented programming:
Introduction to object oriented programming, Programming Basics (keywords, identifiers, variables, operators, classes, objects),Arrays and Strings Functions/ methods (parameter passing techniques)

Chapter 2: OOPs Concepts:
Overview of OOPs Principles, Introduction to classes &objects ,Creation & destruction of objects, Data Members, Member Functions , Constructor & Destructor , Static class member, Friend class and functions, Namespace

UNIT II

Chapter 3: Inheritance:
Introduction and benefits, Abstract class, Aggregation: classes within classes,Access Specifier, Base and Derived class Constructors, Types of Inheritance, Function overriding

Chapter 4: Polymorphism:
Virtual functions, Friend functions, static functions, this pointer

Unit III

Chapter 5: Exception Handling:
Introduction to Exception, Benefits of Exception handling, Try and catch block, Throw statement, Pre-defined exceptions in C++,Writing custom Exception class

Chapter 6: I/O Streams:
C++ Class Hierarchy, File Stream, Text File Handling, Binary File Handling
Error handling during file operations, Overloading << and >> operators

Textbook:

1. Robert Lafore, "Object oriented programming in C++", 4th Edition, Pearson education, 2009. Neural Networks and Deep Learning by Michael Nielsen.

Reference books:

1. Lippman S B, Lajorie J, Moo B E, C++ Primer, 5ed, Addison Wesley, 2013.
2. Herbert Schildt: The Complete Reference C++, 4th Edition, Tata McGraw Hill

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KLE Technological University | Creating Value, Leveraging Knowledge

Program: Electronics Engineering (VLSI Design & Technology)		Semester: VIII
Course Title: MEMS		Course Code: 25EVTE415
L-T-P: 2-0-1	Credits: 3	Contact Hours: 4 hrs/week
ISA Marks: 67	ESA Marks: 33	Total Marks: 100
Teaching Hours: 16 Hrs	Examination Duration: 3 Hrs	

Unit I

Overview of MEMS and Microsystems

Evolution of Microsystems, Miniaturization, Applications of Microsystems in Automotive, Aerospace, Health Care Industry, Industrial Products, Consumer Products and Telecommunications.

Working principles of Microsystems

Micro-sensors: Acoustic wave sensor, Biomedical Sensors and Biosensors, Chemical Sensors Optical Sensors, Pressure Sensors, Thermal Sensors.

Micro-actuation: Actuation Using Thermal Forces, Shape Memory Alloys (SMA), Piezoelectric Crystals and Electrostatic Forces.

Applications of Micro-actuations: Micro-grippers, Micro-motors, Micro-valves, Micro-pumps.

Unit II

Scaling laws in miniaturization: Introduction to scaling, Scaling in Geometry, Rigid-Body Dynamics, Electrostatic Forces, Electromagnetic Forces, Electricity, Fluid Mechanics, Heat Transfer, Numerical problems.

Materials for MEMS and Microsystem: Substrate and Wafers, Active Substrate Materials, Silicon as Substrate Material, Silicon Compounds, Silicon Piezo resistors, Gallium Arsenide, Quartz, Piezoelectric Crystals, Polymers, Packaging Materials.

Unit III

Microsystems Fabrication Processes: Photolithography, Ion Implantation, Diffusion, Oxidation, Chemical Vapor Deposition (CVD), Physical Vapor Deposition (PVD), Etching.

Micro-manufacturing: Bulk Micro-manufacturing,SurfaceMicromachining,The LIGA Process.

Text Book:

1. “MEMS and Microsystems– Design and Manufacture”, Tai-Ran Hsu, TMH Edition 2002.

References:

5. "Micro system Design", Stephen D. Senturia, Kluwer Academic Publishers, 2001.
6. "Foundations of MEMS", Chang Liu, Pearson Edition 2012.
7. "RF MEMS:Theory, Design, and Technology", Gabriel M. Rebeiz, John Wiley & Sons Publication, 2003.

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KLE Technological University | Creating Value, Leveraging Knowledge

Program: Electronics Engineering (VLSI Design & Technology)		Semester: VIII
Course Title: Project Work		Course Code: 25EVTW402
L-T-P: 0-0-11	Credits: 11	Contact Hours: 22 hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: --	Examination Duration: 3 Hrs	

- Smart City
- Connected Cars
- Home Automation
- Health care
- Smart energy
- Automation of Agriculture

Guide lines for selection of a project:

- The project needs to encompass the concepts learnt in the previous semesters, so that the student will learn to integrate, the knowledge base acquired to provide a solution to the defined problem statement of the project work.
- Student can select a project which leads to a product or model or prototype.
- Time plan: Effort to do the project should be between 60-70 Hrs per team, which includes self-study of an individual member (80-100 Hrs) and team work (40-50hrs).
- Learning overhead should be 20-25% of total project development time.

Criteria for group formation:

- 3-4 students in a team.
- Role of teammates: Team lead and members.

Allocation of Guides and Mentors for the projects:

Every Project batch will be allocated with one faculty.

Details of the project batches:

- Number of faculty - members: 50
- Number of students:3-4 students in a team.

Role of a Guide

The primary responsibility of the guide is to help students to understand the meaning and need of various stages in the implementation of the project. At every stage of the project development, guide should help towards its successful completion as per the predefined standards.

How student should carry out a project:

- Define the problem.
- Specify the requirements.

- **Specify the design in the understandable form (Block Diagram, Flowchart, Algorithm, etc).**
- **Analyze the design and identify hardware and software components separately.**
- **Select appropriate simulation tool and development board for the design.**
- **Implement the design.**
- **Optimize the design and generate the results.**
- **Result representation and analysis.**
- **Prepare a document and presentation.**

Report Writing

- **The format for report writing should be downloaded from ftp://10.3.0.3/projects**
- **The report needs to be shown to guide and committee for each review.**
-

Evaluation Scheme

- **Internal semester assessment (ISA)**
- **Evaluation is done based on the evaluation rubrics given in Table 1**
- **Project shall be reviewed and evaluated by the concerned Guide for 50% of the marks.**
- **Project shall be evaluated by the review committee for 50% of the marks.**

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Program: Electronics Engineering (VLSI Design & Technology)		**Semester: VIII**
Course Title: Internship- Training		**Course Code: 25EVTI493**
L-T-P: 0-0-6	**Credits: 6**	**Contact Hours: 12 hrs/week**
ISA Marks: 50	**ESA Marks: 50**	**Total Marks: 100**
Teaching Hours: --	**Examination Duration: 3 Hrs**	

Evaluation parameters for Internship Training

- **Initiative and creativity**
- **Adaptation capacity**
- **Commitment and perseverance**
- **Independence**
- **Handling supervisor's comments and development skills**
- **Time management**
- **Formulation goals, framework project**
- **Theoretical underpinning, use of literature**
- **Use of methods and processing data**
- **Reflection on results**
- **Conclusions and discussion**
- **Presentation skills**

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Program: Electronics Engineering (VLSI Design & Technology)		**Semester: VIII**
Course Title: Internship- Project		**Course Code: 25EVTW494**
L-T-P: 0-0-11	**Credits: 11**	**Contact Hours: 22 hrs/week**
ISA Marks: 50	**ESA Marks: 50**	**Total Marks: 100**
Teaching Hours: --	**Examination Duration: 3 Hrs**	

Evaluation parameters for Internship Project

- **Initiative and creativity**
- **Adaptation capacity**
- **Commitment and perseverance**
- **Independence**
- **Handling supervisor's comments and development skills**
- **Time management**
- **Formulation goals, framework project**
- **Theoretical underpinning, use of literature**
- **Use of methods and processing data**
- **Reflection on results**
- **Conclusions and discussion**
- **Presentation skills**

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Program: Electronics Engineering (VLSI Design & Technology)		Semester: VIII Semester
Course Title: Hardware-Software Co-design		**Course Code: 25EVTO401**
L-T-P: 3-0-0	**Credits: 3**	**Contact Hours: 3Hrs/week**
ISA Marks: 50	**ESA Marks: 50**	**Total Marks: 100**
Teaching Hours: 40Hrs	**Examination Duration:3 Hrs**	

Unit I

Introduction to Hardware Software Codesign Models taxonomy, State-Oriented & Activity Oriented Models, Structure & Data–Oriented Models Architectural Models Introduction to Linux and Ptomley Introduction to Specification Languages Profiling, Benchmarks and SystemC.

Unit II

Polis framework System Partitioning issues Introduction to Low power issues Dynamic Power Management (DVS and DPM). YDS algorithm. Hardware / Software Co-Synthesis Software Power Management. Cache Power Minimization. Design Quality Estimation AMBA Bus Design & LEON3 platform.

Unit III

Compilation Techniques, Device drivers, Case Study

Text Books:

1. Daniel D Gajski, Frank Vahid, Sanjay Narayan, Jie Gong, Specification and Design of Embedded Systems, Prentice Hall, 1994.
2. (T2) Peter Marwedel, Embedded System Design, Kluwer Academic Publishers, 2003, ISBN: 1402076908

Reference Books:

1. G. DeMicheli, R. Ernst and W. Wolf, Readings in Hw/Sw Co-design, M. Kaufmann, 2002.

2. Ahmed A. Jerraya and Jean Mermet eds.: System Level Synthesis, Kluwer 1999.

3. Hardware/Software Codesign. G. DeMicheli and M. Sami (eds.), NATO ASI Series E, Vol. 310, 1996.

4. Sanjaya Kumar, James H. Aylor, Barry W. Johnson, and Wm. A. Wulf. The Codesign of Embedded Systems. Kluwer, 1995

5. IEEE and ACM Transactions. 6. Jorgen Staunstrup, Wayne Wolf, Hardware / Software Co-Design: Principles and Practice, Kluwer Academic, 1997 7. Black David C. Systemc : From The Ground Up

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Program: Electronics Engineering (VLSI Design & Technology)		Semester: VIII Semester
Course Title: System on Chip Design		Course Code: 25EVTO402
L-T-P: 3-0-0	Credits: 3	Contact Hours: 3Hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 40Hrs	Examination Duration:3 Hrs	

Unit I

Chapter No. 1: Introduction

Introduction: Driving Forces for SoC - Components of SoC - Design flow of SoC Hardware/Software nature of SoC - Design Trade-offs - SoC Applications

Chapter No. 2: System Level Design

System-level Design: Processor selection-Concepts in Processor Architecture: Instruction set architecture (ISA), elements in Instruction Handing-Robust processors: Vector processor, VLIW, Superscalar, CISC, RISC—Processor evolution: Soft and Firm processors, Custom Designed processors- on-chip memory.

Unit II

Chapter No. 3: On-chip bus and IP based design

Interconnection: On-chip Buses: basic architecture, topologies, arbitration and protocols, Bus standards: AMBA, Core Connect, Wishbone, Avalon - Network-on chip: Architecture topologies-switching strategies - routing algorithms flow control, Quality-of-Service- Reconfigurability in communication architectures. IP based system design: Introduction to IP Based design, Types of IP, IP across design hierarchy, IP life cycle, Creating and using IP - Technical concerns on IP reuse – IP integration - IP evaluation on FPGA prototypes.

Chapter No. 4: SoC Implementation

SOC implementation: Study of processor IP, Memory IP, wrapper Design - Real-time operating system (RTOS), Peripheral interface and components, High-density FPGAs - EDA tools used for SOC design.

Unit III

Chapter 5: SoC Testing

SOC testing: Manufacturing test of SoC: Core layer, system layer, application layer-P1500 Wrapper Standardization-SoC Test Automation (STAT).

Text Books:

1. Michael J.Flynn, Wayne Luk, “Computer system Design: Systemon-Chip”, Wiley-India, 2012.

2. Sudeep Pasricha, Nikil Dutt, “On Chip Communication Architectures: System on Chip Interconnect”, Morgan Kaufmann Publishers, 2008.

3. W.H.Wolf, “Computers as Components: Principles of Embedded Computing System Design”, Elsevier, 2008.

Reference Books:

1. Patrick Schaumont “A Practical Introduction to Hardware/Software Co-design”, 2nd Edition, Springer, 2012.

2. Lin, Y-L.S. (ed.), “Essential issues in SOC design: designing complex systems-on-chip. Springer, 2006.

3. Wayne Wolf, “Modern VLSI Design: IP Based Design”, Prentice-Hall India, Fourth edition, 2009.

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Program: Electronics Engineering - VLSI Design and Technology		Semester: VIII
Course Title: Advanced DFT for ASIC Design		Course Code: 25EVTE419
L-T-P: 1-0-2	Credits:3	Contact Hours: 5 hrs/week
ISA Marks:67	ESA Marks:33	Total Marks:100
Teaching Hours:16Hrs	Examination Duration:2Hrs	

Week 1: DFT Foundations and Modern Challenges

Lectures:

- Review of basic DFT concepts and fundamentals
- Advancements in modern ASIC testing requirements
- Test economics and the impact of DFT on product quality
- Current industry standards and methodologies

Lab:

- DFT tool setup and environment configuration
- Analysis of ASIC test coverage metrics

Assignment:

- Case study analysis of DFT implementations in commercial ASICs

Week 2: Advanced Scan Architectures

Lectures:

- Multi-mode scan architectures
- Scan compression techniques
- On-chip clock control for scan testing
- Low-power scan techniques

Lab:

- Implementation of compressed scan chains using industry tools
- Analysis of test pattern count reduction

Assignment:

- Design and implementation of a scan compression architecture

Week 3: At-Speed Testing Methodologies

Lectures:

- Clock domain crossing test considerations

- Launch-on-shift vs. launch-on-capture techniques
- Multiple clock domain test strategies
- Path delay fault testing methods

Lab:

- Setting up at-speed test for a sample design
- Transition and path delay fault ATPG

Assignment:

- Analysis and improvement of at-speed test coverage for a given design

Week 4: Memory Testing and BIST

Lectures:

- Memory fault models and test algorithms
- Memory BIST architectures
- Repair strategies and redundancy analysis
- Memory test interfaces and standards

Lab:

- Memory BIST implementation and simulation
- Analysis of memory test coverage

Assignment:

- Design of a memory BIST solution for an embedded SRAM array

Week 5: Boundary Scan and IEEE 1149.x Standards

Lectures:

- IEEE 1149.1 (JTAG) standard in depth
- IEEE 1149.6 for AC-coupled signals
- IEEE 1687 (IJTAG) for instrument access
- Boundary scan test pattern generation

Lab:

- Implementation of JTAG interface and boundary scan cells
- IJTAG network design and implementation

Assignment:

- Development of a comprehensive boundary scan solution for a complex ASIC

Week 6: DFT for Mixed-Signal ICs

Lectures:

- ADC/DAC testing methodologies
- Analog test access mechanisms
- IEEE 1149.4 and mixed-signal test bus
- Loopback testing strategies

Lab:

- Design of test structures for mixed-signal components
- Mixed-signal DFT insertion and analysis

Assignment:

- Development of a test strategy for a mixed-signal subsystem

Week 7: Midterm Project Week

Project:

- Comprehensive DFT implementation for a medium-complexity ASIC
- Test strategy documentation and presentation
- Coverage analysis and optimization

Week 8: Advanced ATPG and Fault Models

Lectures:

- Beyond stuck-at fault models
- Cell-aware fault models
- Small delay defect testing
- Advanced ATPG algorithms and optimizations

Lab:

- Implementation of cell-aware and advanced fault models
- Pattern generation for multiple fault models

Assignment:

- Analysis of test coverage improvement using advanced fault models

Week 9: DFT for Low Power Designs

Lectures:

- Power-aware test strategies
- DFT for power gating architectures
- Testing for power domain isolation
- IEEE 1801 (UPF) integration with DFT

Lab:

- Implementation of power-aware scan insertion
- Analysis of test power consumption

Assignment:

- Development of a low-power test strategy for a multi-power domain design

Week 10: DFT for Advanced SoCs and Multi-Core Designs

Lectures:

- Hierarchical test strategies
- DFT for NoC (Network on Chip) architectures
- Test scheduling and optimization
- Reuse of IP test structures

Lab:

- Implementation of hierarchical test architecture
- Integration of IP-level test structures

Assignment:

- Development of a test strategy for a complex SoC with multiple IP blocks

Week 11: DFT for Emerging Technologies and Final Project

Lectures:

- DFT for 2.5D/3D ICs
- Machine learning applications in testing
- DFT for security (secure scan, anti-tampering)
- Future trends in ASIC testing

Final Project Presentation:

- Comprehensive DFT implementation for a complex ASIC/SoC

- Test coverage analysis and optimization
- Test time and cost evaluation
- Presentation of results and design decisions

Textbook:

1. "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits" by M. Bushnell and V. Agrawal
2. "VLSI Test Principles and Architectures" by L.T. Wang, C.W. Wu, and X. Wen
3. Selected IEEE papers on advanced DFT methodologies
4. Industry white papers on modern DFT implementation

Reference Tools:

- Mentor Graphics Tessent

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