KLE Technological University | Creating Value, Leveraging Knowledge

Curriculum Structure and Curriculum Content for the Academic Year – 2019-23
School /Department: Electronics & Communication Engineering
Program: Bachelor of Engineering

B. V. Bhoomaraddi College Campus, Vidyanagar, Hubballi 580031. Karnataka (India)
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Table of Contents

KLE Technological University | Creating Value, Leveraging Knowledge

Vision and Mission of KLE Technological University

Vision

KLE Technological University will be a national leader in Higher Education–recognised globally for innovative culture, outstanding student experience, research excellence and social impact.

Mission

KLE Technological University is dedicated to teaching that meets highest standards of excellence, generation and application of new knowledge through research and creative endeavours.

The three-fold mission of the University is:

- To offer undergraduate and post-graduate programs with engaged and experiential learning environment enriched by high quality instruction that prepares students to succeed in their lives and professional careers.

- To enable and grow disciplinary and inter-disciplinary areas of research that build on present strengths and future opportunities aligning with areas of national strategic importance and priority.

- To actively engage in the Socio-economic development of the region by contributing our expertise, experience and leadership, to enhance competitiveness and quality of life.

As a unified community of faculty, staff and students, we work together with the spirit of collaboration and partnership to accomplish our mission.

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Vision and Mission Statements of the School / Department

Vision

KLE Tech-School of Electronics and Communication will be well recognized nationally and internationally for excellence in its educational programs, pioneering research and impact on the industry and society.

Mission

1. To create a unique learning environment through rigorous curriculum of theory and practice that develops students' technical, scientific, and professional skills and qualities to succeed in wide range of electronics and computing businesses and occupations.

2. To nurture spirit of innovation and state-of-the-art research to advance the boundaries of disciplinary and interdisciplinary knowledge and its applications.

3. To collaborate within and beyond the discipline to create solutions that benefit humanity and society.

Program Educational Objectives/Program Outcomes and Program-Specific Objectives

Program Educational Objectives -PEO's
1. Graduates will demonstrate peer- recognized technical competency to solve contemporary problems in the analysis, design and development of electronic devices and systems.
2. Graduates will demonstrate leadership and initiative to advance professional and organizational goals with commitment to ethical standards of profession, teamwork and respect for diverse cultural background.
3. Graduates will be engaged in ongoing learning and professional development through pursuing higher education, and self-study.
4. Graduates will be committed to creative practice of engineering and other professions in a responsible manner contributing to the socio-economic development of the society.
Program Outcomes-PO's
PO1: Engineering knowledge: **Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization for the solution of complex engineering problems.**
PO 2: Problem analysis: **Identify, formulate, research literature, and analyse complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.**
PO 3: Design/Development of Solutions: **Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for public health and safety, and cultural, societal, and environmental considerations.**
PO4: Conduct investigations of complex problems: **Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.**
PO 5: Modern tool usage: **Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.**

PO 6: The engineer and society: **Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal, and cultural issues and the consequent responsibilities relevant to the professional engineering practice.**
PO7: Environment and sustainability: **Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.**
PO 8: Ethics: **Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.**
PO 9: Individual and team work: **Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.**
PO 10: Communication: **Communicate effectively on complex engineering activities with the engineering community and with t h e society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.**
PO 11: Project management and finance: **Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.**
PO12: Life-long learning: **Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.**
Program Specific Objectives -PSO's
PSO 1: An ability to apply design principles in the development of hardware and software systems of varying complexity.
PSO 2: Demonstrate the knowledge of the state of art tools and apply for the development of VLSI circuits/systems.
PSO 3: An ability to use appropriate modern techniques for analysis, design and development of Communication components/systems.

Curriculum Structure-Overall

Semester **Total Program**
Credits: 185

Course with course code	I	II	III	IV	V	VI	VII	VIII
	Single Variable Calculus 18EMAB101 (4-1-0)	Multivariable Calculus 18EMAB102 (4-1-0)	BS: Integral Transforms and Statistics 15EMAB203 (4-0-0)	BS: Linear Algebra &Partial Differential Equations 17EMAB208 (4-0-0)	PC10: CMOS VLSI Circuits 19EECC301 (4-0-0)	H3: Professional Aptitude and Logical reasoning. 16EHSC301 (3-0-0)	Wireless and Mobile Networks 22EECC401 (3-0-0)	PSE Elective 6 18EECE (3-0-0)
	Engineering Physics 15EPHB101 (3-0-0)	Engineering Chemistry 15ECHB102 (3-0-0)	PC1: Circuit Analysis 15EECC201 (4-0-0)	ES4: Electromagnetic Fields and Waves 21EECC209 (3-0-0)	PC11: Communication System I 21EECC302 (4-0-0)	PC13: Automotive Electronics 17EECC305 (3-0-0)	PSE Elective 2 18EECE (3-0-0)	Open Elective 18EECE (3-0-0)
	Engineering Mechanics 15ECVF101 (4-0-0)	Problem Solving with Data Structures 18ECSP102 (0-0-3)	PC2: Analog Electronic Circuits 15EECC202 (4-0-0)	PC5: Linear Integrated Circuits 19EECC203 (4-0-0)	PC12: Digital Signal Processing 17EECC303 (4-0-0)		PSE Elective 3 18EECE (3-0-0)	Internship-Training 18EECI493 (0-0-6) Internship-Project 20EEC

								W494 (0-0-11)
	C Programming for Problem solving 18ECSP101 (0-0-3)	Engineering Exploration 15ECRP101 (0-0-3)	PC3: Digital Circuits 19EECC201 (4-0-0)	PC6: Control Systems 15EECC206 (4-0-0)	PC13: Operating System & Embedded Systems Design 17EECC304 (3-0-0)	PC14: Computer Communication Networks 17EECC306 (4-0-0)	PSE Elective 4 18EECE (3-0-0)	Project Work 20EECW402 (0-0-11)
	Basic Electrical Engineering 18EEEF101 (3-0-0)	Basic Electronics 18EECF101 (4-0-0)	PC4: Signals & Systems 19EECC202 (4-0-0)	PC7: ARM Processor & Applications 15EECC207 (3-0-0)	PCL5: Communication and signal processing Lab 17EECP301 (0-0-1)	PC11: Communication System II 21EECC307 (3-0-0)	PSE Elective 5 18EECE (3-0-0)	
	Social Innovation 15EHSP101 (0-1-1)	Basic Mechanical Engg. 15EMEF101 (2-1-0)	PCL1: Digital Circuits Lab 15EECP201 (0-0-1)	PC8: Digital System Design using Verilog 15EECC208 (0-0-2)	PCL6: RTOS Lab 17EECP302 (0-0-1)	PSE Elective 1 17EECEXXX (3-0-0)	P3: Senior Design Project 20EECW401 (0-0-6)	

	Engineering Physics Lab 16EPHP101 (0-0-1)	Professional Communication 15EHSH101 (1-1-0)	PCL2: Analog Electronic Circuits Lab 15EECP202 (0-0-1)	PCL3: Data acquisition and controls Lab 15EECP203 (0-0-1)	PCLx: CMOS VLSI Circuits Lab 19EECP301 (0-0-1)	PCL7: Computer Communication Networks Lab 17EECP303 (0-0-1)	CIPE & EVS 15EHSA401 (2-0-0)	
			ES2: Microcontroller Architecture & Programming 21EECF202 (0-0-3) C Programming (Dip)18EECF204 (0-0-3)	PCL4: ARM Microcontroller Lab 15EECP204 (0-0-1)	PC15: Machine Learning 17EECC307 (2-0-1)	PCL8: Automotive Electronics Lab 22EECP304 (0-0-1)		

				PCL3: Data Structure Applications Lab 21EECF201 (0-0-2) PCL3: Data Structure Using C Lab(Diploma) 21EECF203 (0-0-3)	P1: Mini Project 17EECW301(0-0-3)	P2: Minor Project 17EECW302 (0-0-6)		
Credits	21	23	24	24	24	24	24	21

FIRST SEMESTER B E PROGRAMSCHEME FOR 2019-2020

Electrical Science Stream

This stream comprises of Departments of Electrical Engg / Electronics & communication Engg /Computer Science and Engg.

No	Code	Course	Category	L-T-P	Credits	Contact Hours	CIE	SEE	Total	Exam Duration
1	18EMAB101	Single Variable Calculus	BS	4-1-0	5	6	50	50	100	3 hrs
2	15EPHB101	Engineering Physics	BS	3-0-0	3	3	50	50	100	3 hrs
3	15ECVF101	Engineering Mechanics	ES	4-0-0	4	4	50	50	100	3 hrs
4	18ECSP101	C Programming for Problem solving	ES	0-0-3	3	6	80	20	100	3 hrs
5	18EEEF101	Basic Electrical Engineering	ES	3-0-0	3	3	50	50	100	3 hrs
6	15EHSP101	Social Innovation	HSS	0-1-1	2	3	50	50	100	1.5hrs
7	16EPHP101	Engineering Physics Lab	BS	0-0-1	1	2	80	20	100	3 hrs
Total				**14-2-5**	**21**	**27**				

SECOND SEMESTER B E PROGRAMSCHEME FOR 2019-20

Electrical Science Stream

This stream comprises of Departments of Electrical Engg / Electronics & communication Engg /Computer Science and Engg.

No	Code	Course	Catego	L-T-P	Credit	Contact Hours	ISA	ESA	Total	Exam Duratio
1	18EMAB102	Multivariable Calculus	BS	4-1-0	5	6	50	50	100	3 hrs
2	15ECHB102	Engineering Chemistry	BS	3-0-0	3	3	50	50	100	3 hrs
3	18ECSP102	Problem Solving with Data Structures	ES	0-0-3	3	6	80	20	100	3 hrs
4	15ECRP101	Engineering Exploration	ES	0-0-3	3	6	80	20	100	3 hrs
5	**18EECF101**	**Basic Electronics**	ES	4-0-0	4	4	50	50	100	3 hrs
6	15EMEF101	Basic Mechanical Engg.	ES	2-1-0	3	4	50	50	100	3 hrs
7	15EHSH101	Professional Communication	HSS	1-1-0	2	3	50	50	100	1.5 hrs
Total				**15-2-6**	**23**	**32**				

Semester: III

No	Code	Course	Categor	L-T-P	Credi	Conta Hours	ISA	ESA	Total	Exam Duration
1	15EMAB203	BS: Integral Transforms and Statistics	BS	4-0-0	4	4	50	50	100	3 hours
2	15EECC201	PC1: Circuit Analysis	PC	4-0-0	4	4	50	50	100	3 hours
3	15EECC202	PC2: Analog Electronic Circuits	PC	4-0-0	4	4	50	50	100	3 hours
4	19EECC201	PC3: Digital Circuits	PC	4-0-0	4	4	50	50	100	3 hours
5	19EECC202	PC4: Signals & Systems	ES	4-0-0	4	4	50	50	100	2 hours
6	15EECP201	PCL1: Digital Circuits Lab	PC	0-0-1	1	2	80	20	100	2 hours
7	15EECP202	PCL2: Analog Electronic Circuits Lab	PC	0-0-1	1	2	80	20	100	2 hours
8	15EECF202 18EECF204	ES2: Microcontroller Architecture & Programming C Programming	ES	0-0-2	2	4	80	20	100	2 hours
TOTAL				**20-0-4**	**24**	**28**	**490**	**310**	**800**	

ISA: In Semester Assessment **ESA**: End Semester Assessment **L**: Lecture **T**: Tutorials **P**: Practical

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Semester: IV

No	Code	Course	Category	L-T-P	Credi	Conta Hours	ISA	ESA	Total	Exam Duration
1.	17EMAB208	BS: Linear Algebra &Partial Differential Equations	BS	4-0-0	4	4	50	50	100	3 hours
2.	18EECC209	ES4: Electromagnetic Fields and Waves	PC	3-0-0	3	3	50	50	100	3 hours
3.	19EECC203	PC5: Linear Integrated Circuits	PC	4-0-0	4	4	50	50	100	3 hours
4.	15EECC206	PC6: Control Systems	PC	4-0-0	4	4	50	50	100	3 hours
5.	15EECC207	PC7: ARM Processor & Applications	PC	3-0-0	3	3	50	50	100	3 hours
6.	15EECC208	PC8: Digital System Design using Verilog	PC	0-0-2	2	4	80	20	100	2 hours
7.	15EECP203	PCL3: Data acquisition and controls Lab	PC	0-0-1	1	2	80	20	100	2 hours
8.	15EECP204	PCL4: ARM Microcontroller Lab	PC	0-0-1	1	2	80	20	100	2 hours
9.	19EECF201 19EECF202	PCL3: Data Structure Applications Lab PCL3: Data Structure Lab(Diploma)	ES	0-0-2	2	4	80	20	100	2 hours
TOTAL				**18-0-6**	**24**	**28**	**570**	**330**	**900**	

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Semester: V

No	Code	Course	Category	L-T-P	Credit	Contact Hours	ISA	ESA	Total	Exam Duration
1	19EECC301	PC10:CMOS VLSI Circuits	PC	4-0-0	4	4	50	50	100	3 hours
2	21EECC302	PC11: Communication System I	PC	4-0-0	4	4	50	50	100	3 hours
3	17EECC303	PC12: Digital Signal Processing	PC	4-0-0	4	4	50	50	100	3 hours
4	17EECC304	PC13: Operating System & Embedded Systems Design	PC	3-0-0	3	3	50	50	100	3 hours
5	17EECP301	PCL5: Communication and signal processing Lab	PC	0-0-1	1	2	80	20	100	2 hours
6	17EECP302	PCL6: RTOS Lab	PC	0-0-1	1	2	80	20	100	2 hours
7	19EECP301	PCLx: CMOS VLSI Circuits Lab	PC	0-0-1	1	2	80	20	100	2 hours
8	17EECC307	PC15: Machine Learning	PC	2-0-1	3	4	50	50	100	3 hours
9	17EECW301	P1: Mini Project	PW	0-0-3	3	6	50	50	100	2 hours
TOTAL				17-0-7	**24**	**31**	**540**	**360**	**900**	

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Semester: VI

No	Code	Course	Category	L-T-P	Credit	Contact Hours	ISA	ESA	Total	Exam Duration
1	16EHSC301	H3: Professional Aptitude and Logical reasoning.	HC	3-0-0	3	3	50	50	100	3 hours
2	17EECC305	PC13:Automotive Electronics	PC	3-0-0	3	3	50	50	100	3 hours
3	17EECC306	PC14:Computer Communication Networks	PC	4-0-0	4	4	50	50	100	3 hours
4	21EECC307	PC11: Communication System II	PC	3-0-0	3	3	50	50	100	3 hours
5	17EECEXXX	PSE Elective 1	PE	3-0-0	3	3	50	50	100	3 hours
6	17EECP303	PCL7: Computer Communication Networks Lab	PC	0-0-1	1	2	80	20	100	2 hours
7	17EECP304	PCL8: Automotive Electronics Lab	PC	0-0-1	1	2	80	20	100	2 hours
8	17EECW302	P2: Minor Project	PW	0-0-6	6	12	50	50	100	2 hours
TOTAL				16-0-8	**24**	**32**	**460**	**340**	**800**	

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Elective VI (Batch 2019-23)

Semester: VI										
No	**Code**	**Course:** PSE1: Elective	**Category**	**L-T-P**	**Credit**	**Contact Hours**	**ISA**	**ESA**	**Total**	**Exam Duration**
PSE Elective 1	17EECE301	Analog Circuits Design	PSE	0-0-3	3	6	100		100	3Hours
	19EECE322	Introduction to Deep Learning		2-0-1		4	50	50		
	17EECE302	Advanced Digital Logic Design		0-0-3		3	100			
	17EECE307	Internet of Things		2-0-1		4	50	50		
	21EECE308	Information Theory and Coding		3-0-0		3	50	50		
	17EECE310	Embedded Intelligence Systems		0-0-3		9	80	20		
	20EECE340	Multi core Architecture & Programming		2-0-1		4	50	50		
	18EECE421	OOPS using C++		2-0-1		4	50	50		

Semester: VII

No	Code	Course	Category	L-T-P	Credits	Contact Hours	ISA	ESA	Total	Exam Duration
1	22EECC401	PC16: Wireless & Mobile Communication	PSC	3-0-0	3	3	50	50	100	3 hours
2	18EECE	PSE Elective 1	PSE	3-0-0	3	3	50	50	100	3 hours
3	18EECE	PSE Elective 2	PSE	3-0-0	3	3	50	50	100	3 hours
4	18EECE	PSE Elective 3	PSE	3-0-0	3	3	50	50	100	3 hours
5	18EECE	PSE Elective 4	PSE	3-0-0	3	3	50	50	100	3 hours
6	20EECW401	P3: Senior Design Project	PW	0-0-6	6	12	50	50	100	3 hours
7	15EHSA401	CIPE	M	2-0-0		2	50	50	100	3 hours
TOTAL				**15-0-6**	**21**	**29**	**350**	**350**	**700**	

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Semester: VII (2019-23 Batch)

Subject		Subject code	Theory	Practical	Credits	Remark
Group-I Electives	Fabrication Techniques for MEMs-based sensors **(Swayam)**	22EECE430	0	3	3	**Select any one subject from Group-I**
	Cryptography & Network Security **(Swayam)**	22EECE431	0	3		
	Phase-locked loops**(Swayam)**	22EECE432	0	3		
	Computer Graphics**(IITD-Online)**	21EECE425	0	3		
	Advanced Computer Graphics(**IITD + KLE Tech**)	22EECE433	0	3		
	Advanced Computer Vision(**IITD + KLE Tech**)	22EECE434	0	3		
Group-II Electives	Advanced Digital Logic verification	18EECE418	0	3	9	**Select any Three subject from Group-II**
	Multimedia Communication	18EECE410	3	0		
	Physical Design-Analog	18EECE419	0	3		
	OOPS with C++	18EECE421	2	1		
	CMOS ASIC Design	18EECE420	0	3		
	Embedded Linux	18EECE405	0	3		
	Microwave & Antennas	18EECE411	3	0		
	AUTOSAR	20EECE406	3	0		
	Testing & Characterization	19EECE403	3	0		

No	Code	Course: PSE: Elective	Category	L-T-P	Credits	Contact Hours	ESA	ISA	Total	Exam Duration
1.	19EECE416	Biosensor	PSE	0-0-3	3	3	-	100	100	3Hours
2.	18EECE418	Advanced Digital Logic verification		0-0-3		6	-	100		

3.	18EECE410	Multimedia Communication		3-0-0		3	50	50		
4.	18EECE419	Physical Design-Analog		0-0-3		6	-	100		
5.	18EECE409	Design and Analysis of Algorithm		0-0-3		3	50	50		
6.	18EECE420	CMOS ASIC Design		0-0-3		6	-	100		
7.	18EECE405	Embedded Linux		0-0-3		3	50	50		
8.	18EECE411	Microwave & Antennas		3-0-0		3	50	50		
9.	20EECE406	AUTOSAR		3-0-0		3	50	50		
10.	18EECE415	Cryptography & Network Security		3-0-0		3	50	50		
11.	19EECE403	Testing & Characterization		0-0-3		6	-	100		
12.	17EECE310	Embedded Intelligent Systems		0-0-3		6	80	20		
13.	21EECE421	RF VLSI		3-0-0		3	50	50		
14.	21EECE422	Speech Processing		3-0-0		3	50	50		
15.	21EECE423	CAD for VLSI		3-0-0		3	50	50		
16.	21EECE424	System on Chip Design		3-0-0		3	50	50		
17.	22EECE423	Power Management Integrated Circuit		3-0-0		3	50	50		
18.	22EECE424	Virtualization and Cloud Computing		3-0-0		3	50	50		

Semester: VIII

No	Code	Course	Category	L-T-P	Internship	Credits	Contact Hours	ISA	ESA	Total	Exam Duration
1	18EECE	PSE Elective 5	PSE	3-0-0	6-0-0	3	3	50	50	100	3 hours
2	18EECE	Open Elective 1	OE	3-0-0		3	3	50	50	100	3 hours
3	20EECW402	Project Work	PRJ	0-0-11		11	22	50	50	100	3 hours
TOTAL				**6-0-11**		**17**	**28**	**150**	**150**	**300**	

Internship- Training: 18EECI493 – 0-0-6, ISA: 50 ESA: 50

Internship- Project: 20EECW494-- 0-0-11, ISA: 50 ESA: 50

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No	Code	Course: PSE5: Elective	Categor	L-T-P	Credit	Contact Hours	ISA	ESA	Total	Exam Duration
1.	18EECE414	Digital Image Processing		3-0-0	3	3				
	18EECE403	MEMS		3-0-0	3	3				
	19EECE422	Introduction to Deep Learning		2-0-1	3	4				
	18EECE402	Analog and Mixed Mode Circuits		3-0-0	3	3				
	20EECE430	Multi core Architecture & Programming		2-0-1	3	4				

No	Code	Course: OE1s: Open Elective	Categor	L-T-P	Credit	Contact Hours	ISA	ESA	Total	Exam Duration
OE2	18EECO403	Automotive Electronics	OE	3-0-0	3	3	50	50	100	3Hours
	18EECO404	Embedded System		3-0-0						

Program: I Semester Bachelor of Engineering (Electronics & Communication Engineering)			Teaching Hours
Course Title: Basic Electronics(Mechanical Science)		Course Code: 18EECF101	
L-T-P: 4-0-0	Credits: 4	Contact Hours: 4Hrs/week	
ISA Marks: 50	ESA Marks: 50	Total Marks: 100	
Teaching Hours: 50Hrs	Examination Duration: 3 Hrs		
Unit I **Chapter 1: Overview of Electronics in Mechanical Engineering** Definition & overview of Mechatronics, Mechatronics and Design Innovation, Mechatronics and Manufacturing, Mechatronics and Education; Typical Mechatronics Components; Sensors and Transducers.			03
Chapter 2: Semiconductor Devices and Applications: PN junction diode, characteristics and parameters, diode approximations, half wave rectifier, full wave bridge rectifier, full wave bridge rectifier capacitor filter, Zener diode, Voltage regulator design, BJT, Darlington Pair, JFET, MOSFET, UJT, SCR.			10
Chapter 3: Operational Amplifiers: Ideal op-amp characteristics, op-amp applications: Comparator, Inverting amplifier, Non-inverting amplifier, Voltage follower, Integration, Differentiation, Adder, Subtractor and numerical as applicable.			08
Unit II **Chapter 4: Digital Logic:** Digital Number system: Binary & Hexadecimal number systems, Conversion, BCD Number system, Gray code, Data word representation, Binary Arithmetic, Boolean Algebra, Logic gates, Combinational & Sequential circuits, Adders, Flip-Flops, Registers, Counters, Multiplexer. **Introduction to Digital Electronics (Text-2):** Introduction, Switching and Logic Levels using circuits, Digital Waveform (Sections 9.1to 9.3). Number system: Binary, Octal Decimal and Hexadecimal, Inter Conversion, BCD Number system, Gray code, Data word representation, Binary Arithmetic, Boolean Algebra: Laws, rules & theorems of Boolean algebra, Sum of products form (SOP), products of sum form (POS) of Boolean functions. Study of Karnaugh Maps (K-maps) for 2, 3 & 4 variables only. Logic gates, Adders, Encoder, Decoder, Multiplexer and DE multiplexer. Combinational & Sequential circuits, Latches and Flip-Flops(SR, JK, D, T),			13

Chapter 5: Sensors and Transducers: Introduction, Classification of sensors and transducers, Contact type – Mechanical switches, Non-contact type - proximity sensors & Hall sensors, principle of working of light sensors, Future Challenges	**06**
Unit – III **Chapter 6: Signal Conditioning:** Analog & Digital signals, Digital to Analog Conversion, R-2R DAC, Analog to Digital Conversion, SAR ADC, Data Acquisition.	**06**
Chapter 7: Case Studies of Mechatronic Systems: Automatic Camera, Drilling Machine, Bar code reader.	**04**

Text Book

1. David A Bell, “Electronic devices and Circuits” , PHI New Delhi, 2004.
2. Morris Mano, “Digital logic and Computer design” 21st Indian print Prentice Hall India, 2000.
3. W.Bolton, "Mechatronics - Electronic Control Systems in Mechanical and Electrical Engineering", 3rd edition Pearson Education, 2005.
4. David Bradley and David W., “Mechatronics in Action”, 2nd edition, Springer, 2010

References

1. David G Alciatore, Michael B Histand, “Introduction to Mechatronics and Measurement Systems”, TMH 3rd edition, 2007.
2. K.A Krishnamurthy and M.R.Raghuveer, “Electrical, Electronics and Computer Engineering for Scientist and Engineers”, Second Edition New Age International Publishers, Wiley Eastern, 2001.
3. P. Malvino, “Electronic Principles” Sixth edition Tata McGraw Hill, 1999.
4. Floyd, “Digital fundamentals” Third Edition Prentice Hall India, 2001
5. Boylestead Nashelsky, “Electronic devices & Circuit theory” Sixth Edition Prentice Hall India, 2000. RamakantGayekawad “Operational Amplifiers & applications” 3rd Edition, PHI, 2000.

Back to II Sem

Program: I Semester Bachelor of Engineering (Electronics & Communication Engineering)		
Course Title: Basic Electronics(Electrical Science)		Course Code: 18EECF102
L-T-P: 4-0-0	Credits: 4	Contact Hours: 4Hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 50Hrs	Examination Duration: 3 Hrs	

Content	Hrs
Unit – 1	
Chapter 1: Basic components, devices and Applications Diode: PN junction characteristics; modeling as a circuit element, ideal and practical diode. AC to DC converter: Half wave and full wave rectifier (center tap and bridge), capacitor filter and its analysis, numerical examples. Zener diode and its applications (Voltage reference and voltage regulator). Realization of simple logic gates like AND and OR gates.	09 hrs
Chapter 2: Transistor BJT, transistor voltages and currents, Signal amplifier (Fixed bias, Collector base bias, Voltage divider bias, CE configuration). DC load line. Voltage, current and power gains. Transistor as a switch: NOT Gate, Basic (DTL) NAND gate. Transistor as a Small Signal Amplifier (Single Stage and Two Stage RC-coupled Amplifier).	11 hrs
Unit – 2	
Chapter 3: Digital Logic Number systems: Decimal, Binary, Octal and Hexadecimal number systems, Conversions, Binary Operations- Addition and subtraction in binary number systems. Logic gates: Realization of simple logic functions using basic gates (AND, OR, NOT), Realization using universal gates (NAND, NOR). Boolean algebra: Theorems and postulates, DeMorgan's Theorems, simplification of logical expressions, Karnaugh Maps, Use of Karnaugh Maps to Minimize Boolean Expressions (2 Variables, 3 Variables and 4 Variables), Design of Half Adder and Full Adder, Parallel Adder using full adders..	13 hrs
Chapter 4: Operational Amplifier OPAMP characteristics (ideal and practical). Concept of positive and negative feedback (At zero frequency). Linear and non-linear applications: Inverting amplifier, Non inverting amplifier, Voltage follower, Integration, Differentiation, Adder, Subtractor, ZCD and Comparator.	07 hrs
Unit – 3	
Chapter 5: Communication Systems Basic block diagram of communication system, types of modulation. Amplitude modulation: Time-Domain description, Frequency-Domain description. Generation of AM wave: square law modulator. Detection of AM waves: envelope detector. Double side band suppressed carrier modulation (DSBSC), Generation of DSBSC wave: balanced modulator, Super heterodyne principle.	07 hrs

Chapter 6: Linear Power Supply, UPS & CRO Working principle of linear power supply, UPS and CRO. Measurement of amplitude, frequency and phase of a given signal.	03 hrs

Text Book

1. David A Bell, Electronic devices and Circuits, PHI New Delhi, 2004
2. K.A Krishnamurthy and M.R.Raghuveer, Electrical, Electronics and Computer Engineering for Scientist and Engineers, 2, New Age International Publishers, 2001
3. A.P. Malvino, Electronic Principles, Tata McGraw Hill, 1999

References

1. George Kennedy, Electronic Communication Systems, 4, Tata McGraw Hill, 2000
2. Morris Mano, Digital logic and Computer design, 21st Indian print Prentice Hall India, 2000
3. Floyd, Digital fundamentals, 3, Prentice Hall India, 2001
4. Ramakant Gaikawad , Operational Amplifiers & applications, 3, PHI, 2000

Back to II Sem

Program: III Semester Bachelor of Engineering (Electronics & Communication Engineering)			Teaching Hours
Course Title: Integral transforms and Statistics		Course Code: 15EMAB203	
L-T-P: 4-0-0	Credits: 04	Contact Hours: 4Hrs/week	
ISA Marks: 50	ESA Marks: 50	Total Marks: 100	
Teaching Hours: 50Hrs	Examination Duration: 3 Hrs		
Unit I **Chapter 1. Laplace Transforms** Definition, transforms of elementary functions- transforms of derivatives and integrals- Properties. Periodic functions, Unit step functions and Unit impulse functions. Inverse Transforms- properties- Convolution Theorem. Initial and Final value theorems, examples; Applications to differential equations, Circuit equations			10
Chapter 2: Probability Definition of probability, conditional probability, Baye's rule, Chebyshev's inequality, random variables- PDF-CDF- Probability Distributions: Binomial, Poisson, Exponential, Uniform, and Normal			10
Unit II **Chapter 3: Regression:** Introduction to method of least squares, fitting of curves y=a+bx, $y = ab^x$, correlation and regression. Engineering problems.			05
Chapter 4: Fourier Series Complex Sinusoids, Fourier series representations of four classes of signals, Periodic Signals: Fourier Series representations, Derivation of Complex Co-efficients of Exponential Fourier Series and Examples. Convergence of Fourier Series. Amplitude and phase spectra of a periodic signal. Properties of Fourier Series (with proof): Linearity, Symmetry Properties, Time shift, Frequency Shift, Scaling, Time differential differentiation coefficients, Time domain Convolution, Multiplication Theorem, Parseval's theorem and Examples on these properties.			08
Chapter 6: Fourier Transform: Fourier representation of non-periodic signals, Magnitude and phase spectra. Properties of Fourier Transform: Linearity, Symmetry Properties, Time shift, Frequency Shift, Scaling, Time differential differentiation coefficients, Time domain Convolution, Multiplication Theorem, Parseval's theorem and Examples on these properties.			07
Unit III **Chapter 6: Random Process:** 1. Introduction to Joint Probability Distributions, marginal distribution, joint pdf and cdf, mean, variance, covariance, correlation. 2. Introduction to Random process, stationary process, mean, correlation and covariance function, autocorrelation function, cross correlation, Power spectral Density: properties of the spectral density; Gaussian Process: Properties of Gaussian process.			10

Text Books

1. Kreyszig E., Advanced Engineering Mathematics, 10th edition, Wiley, 2015
2. Gupta S C and Kapoor V K, Fundamentals of Mathematical Statistics, 11th edition, Sultan Chand & Sons, 2018
3. Walpole and Myers, Probability and Statistics for Engineers and Scientists, ; 9thedition , Pearson Education India,2013.

References

1.Simon Haykin, Barry Van Veen, Signals and Systems Wiley; Second edition ,2007

2.J. Susan Milton, Jesse C. Arnold, Introduction to Probability and Statistics: Principles and Applications for Engineering and the Computing Sciences, 4th edition, TATA McGraw-Hill Edition, 2017

3.Ian Glover & Peter Grant, Digital Communications, 3rd edition, Pearson 2009.

Back to III Sem

Program: III Semester Bachelor of Engineering (Electronics & Communication Engineering)			Teaching Hours
Course Title: Circuit Analysis		**Course Code: 15EECC201**	
L-T-P-SS: 4-0-0	**Credits: 4**	**Contact Hours: 4Hrs/week**	
ISA: Marks: 50	**ESA: Marks: 50**	**Total Marks: 100**	
Teaching Hours: 50Hrs	**Examination Duration:3 Hrs**		
Unit I **Chapter 1: Basics** Active and passive circuit elements, Voltage & current sources, Resistive networks, Nodal Analysis, Super node, Mesh Analysis, Super mesh, Star – Delta Transformation. [Text 1: Chapter 4,5, 7]			**06**
Chapter 2: Network Theorems Homogeneity, Superposition and Linearity, Thevenin's& Norton's Theorems, Maximum Power Transfer Theorem, Miller's theorem, Reciprocity principle. [Text 1 : Chapter 5]			**08**
Chapter 3: Network topologies Graph of a network, Concept of tree and co-tree, incidence matrix, tie set and cut set schedules, Formulation of Equilibrium equations in matrix form, Solution of resistive networks. [Text 1: Chapter 5]			**04**
Unit II **Chapter 4: Two Port Networks** Two port variables, Z,Y, H,G, A- Parameter representations, Input and output impedance calculation, Series, Parallel and Cascade network connections, and their (suitable) models. [Text 2 : Chapter 11]			**06**
Chapter 5: Time and Frequency Domain Representation of Circuits Order of a system, Concept of Time constant, System Governing equation, System Characteristic equation, Initial conditions, Transfer Functions (Fourier and Laplace domain representation) [Text 2: Chapter 4]			**06**
Chapter 6: First order circuits Transient response of R-C and R-L networks (with Initial conditions) Concept of phasor, Phasor diagrams, Frequency response characteristics, Polar plots R-C , R-L circuits as differentiator and integrator models, time and frequency domain responses R-C , R-L circuits as Low pass and high pass filters [Text 2: Chapter 5, Text 1: Chapter 8,9,10]			**08**
Unit III **Chapter 7: Higher order circuits** HigherorderR-C,R-L,andR-L-Cnetworks,timedomainandfrequencydomainrepresentation, Phasor diagrams, Polar and logarithmic plots, Series R-L-C circuit, Transient response, Damping factor, Quality factor, Frequency response curve, Peaking of frequency curve and its relation to damping factor, Resonance Parallel, R-L-C circuit, Tank circuit, Resonance, Quality factor and Bandwidth			**12**

[Text 2: Chapter 7,8]	

Text Books

1. W H Hayt, J E Kemmerly, S M Durban, "Engineering Circuit Analysis"McGraw Hill Education; Eighth edition ,2013
2. M E. Van Valkenburg, Network Analysis, Third edition Pearson Education, 2019

Reference

1. Joseph Edminister, Mahmood Nahavi, Electric Circuits, 5th edition, McGraw Hill Education, 2017
2. V. K. Aatre, —Network Theory and Filter Design,3rd edition, New Age International Private Limited,2014

Back to III Sem

Program: III Semester Bachelor of Engineering (Electronics & Communication Engineering)			
Course Title: Analog Electronic Circuits		**Course Code: 15EECC202**	**Teaching Hours**
L-T-P: 4-0-0	**Credits: 4**	**Contact Hours: 4Hrs/week**	
ISA Marks: 50	**ESA Marks: 50**	**Total Marks: 100**	
Teaching Hours: 50Hrs	**Examination Duration: 3 Hrs**		
Unit I **Chapter 1: Applications of a Junction diode:** Recap of diode models: piece-wise linear model, constant voltage drop model, ideal diode model, small signal model. Applications of diodes as a Clipping circuit and clamping circuits Voltage dubler. (T1 : 2.2,2.3.1 to 2.3.8,2.6.1to 2.6.3.)			**06**
Chapter No. 2. Bipolar junction transistors. The common emitter characteristics, Dependence of Ic on the collector voltage-the early effect large signal operation-the transfer characteristics, the amplifier gain, operation as a switch. DC load line and bias point, base- bias, collector to base bias, voltage divider, comparison of bias circuit, small signal models of bipolar transistors, two port modeling of amplifiers, ac analysis of BJT circuits-coupling and bypass capacitor, Common emitter circuit analysis, CE circuit with un-bypassed emitter resistor. (T1: 3.1.1, 3.2.1,3.2.2, 3.2.3, 3.2.4, 3.3.1, 3.3.2, 3.3.4)			**07**
Chapter 3: MOSFETs structure and physical operation: Device structure, operation with no gate voltage, creating a channel for current flow, applying small vds, operation as vds is increased, derivation of the id-vds relationship, the P-channel MOSFET, complementary MOS or CMOS, operating the mos transistor in the sub threshold region. Current-voltage characteristics: circuit symbol, the id vsvds characteristics, finite output resistance in saturation, characteristics of the p-channel MOSFET, the role of the substrate-the body effect, temperature effects, breakdown and input protection. MOSFET circuits at DC. **(T1: 4.1, 4.2 ;4.3)**			**07**
Unit II **Chapter 4: Biasing of MOSFETs** MOSFET circuits at DC. Biasing in mos amplifier circuits,By fixing VGS By fixing VG;With drain to gate feedback resistor; Constant current source biasing and Numerical **(T1:4.3)**			**08**
Chapter 5: MOSFET amplifiers: Biasing in mos amplifier circuits, small signal operation and models, single stage MOS amplifiers, the MOSFET internal capacitance and high frequency model, frequency response of CS amplifier. (CD and CG),Cascade Connection: Implications on gain and Bandwidth **(T1:4.4,4.5, 4.6.1 to 4.6.7 ; 4.7.1, 4.7.2, 4.7.3, 4.7.5, 4.7.6, 4.7.7;4.8.1,4.8.2, 4.8.3,4.8.4, 4.9.1 to 4.9.3)**			**12**

Unit III **Chapter 6: Feedback Amplifiers:** General feedback structure (Block schematic), Feedback desensitivity factor, positive and negative feedback Nyquist stability Criterion, RC phase shift oscillator, wein bridge Oscr, merits of negative feedback, feedback topologies: series-shunt feedback amplifier, series-series feedback amplifier, and shunt-shunt and shunt-series feedback amplifier with examples (T1:7.1 to 7.6)	**05**
Chapter 7: Large Signal Amplifiers: Classification of amplifiers: (A, B, AB and C); Transformer coupled amplifier, push-pull amplifier Transistor case and heat sink. (T1:12.1 to 12.6;12.8.4)	**05**

Text Books

1. A.S. Sedra& K.C. Smith, "Microelectronic Circuits",7th edition, Oxford University Press, 2017

Reference

1. JacobMillman and Christos Halkias,-Integrated Electronics "McGraw Hill Education, 2nd edition 2017
2. DavidA.Bell,-Electronic Devices and Circuits, Oxford Fifth edition 2008
3. Grey,Hurst,Lewis and Meyer,-Analysis and design of analog integrated circuits,Wiley,5th edition 2009
4. Thomas L.Floyd,-Electronic devices ,Pearson, 10th edition, 2018
5. Richard R. Spencer & Mohammed S. Ghousi, — Introduction to Electronic Circuit Design‖, Pearson Education,2003
6. J. Millman& A. Grabel, "Microelectronics"-2nd edition, McGraw Hill,2017
7. Behzad Razavi,-Fundamentals of Microelectronics, 2nd edition Wiley;2013

Back to III Sem

Program: III Semester Bachelor of Engineering (Electronics & Communication Engineering)			Teaching Hours
Course Title: Digital Circuits		Course Code: 19EECC201	
L-T-P: 4-0-0	Credits: 4	Contact Hours: 4Hrs/week	
ISA Marks: 50	ESA Marks: 50	Total Marks: 100	
Teaching Hours: 50 Hrs	Examination Duration: 3 Hrs		
Unit-I **Chapter No. 1. Logic Families** Logic levels, output switching times, fan-in and fan-out, comparison of logic families			03
Chapter No. 2. Principles of Combinational Logic Definition of combinational logic, canonical forms, Generation of switching equations from truth tables, Karnaugh maps-3,4 variables, Incompletely specified functions(Don't care terms),Simplifying Maxterm equations, Quine-McCluskey minimization technique- Quine-McCluskey using don't care terms, Reduced Prime Implicant Tables.			10
Chapter No. 3. Analysis and design of combinational logic General approach, Decoders-BCD decoders, Encoders, Digital multiplexers- Using multiplexers as Boolean function generators. Adders and sub tractors-Cascading full adders, Look ahead carry adders, Binary comparators.			08
Unit-II **Chapter No. 4. Introduction to Sequential Circuits** Basic Bistable Element, Latches, A SR Latch, Application of SR Latch, A Switch De bouncer, The SR Latch, The gated SR Latch, The gated D Latch, The Master-Slave Flip-Flops (Pulse-Triggered Flip-Flops): The Master-Slave SR Flip-Flops, The Master-Slave JK Flip-Flop, Edge Triggered Flip- Flop: The Positive Edge-Triggered D Flip-Flop, Negative-Edge Triggered D Flip-Flop; Characteristic Equations			10
Chapter No. 5. Analysis of Sequential Circuits Registers and Counters, Binary Ripple Counters, Synchronous Binary counters, Ring and Johnson Counters, Design of a Synchronous counters, Design of a Synchronous Mod-n Counter using clocked JK Flip-Flops Design of a Synchronous Mod-n Counter using clocked D, T or SR Flip-Flops.			10
Unit-III **Chapter No. 6. Sequential Circuit Design** Introduction to Sequential Circuit Design, Mealy and Moore Models, State Machine notations, Synchronous Sequential Circuit Analysis, Construction of state Diagrams and counter design.			05
Chapter No. 7. Introduction to memories Introduction and role of memory in a computer system, memory types and terminology, Read Only memory, MROM, PROM, EPROM, EEPROM, Random access memory, SRAM, DRAM, NVRAM.			04

Text Books

1. Donald D Givone, Digital Principles and Design,McGraw Hill Education ,2017
2. John M Yarbrough, Digital Logic Applications and Design,1st editionCengage Learning, 2006
3. A AnandKumar , Fundamentals of digital circuits 4th Revised edition, PHI ,2016

References

1. Charles H Roth, Fundamentals of Logic Design,7th edition ,Cengage Learning, 2015
2. ZviKohavi, Switching and Finite Automata Theory Cambridge University Press; 3 edition October 2009
3. R.D. Sudhaker Samuel, Logic Design, Pearson Education ,2010
4. R P Jain, Modern Digital Electronics , 4th edition, McGraw Hill Education, 2009

Back to III Sem

Program: III Semester Bachelor of Engineering (Electronics & Communication Engineering)			Teaching Hours
Course Title: Signals and Systems		Course Code: 19EECC202	
L-T-P: 4-0-0	Credits: 4	Contact Hours: 4Hrs/week	
ISA Marks: 50	ESA Marks: 50	Total Marks: 100	
Teaching Hours: 50Hrs	Examination Duration: 3 Hrs		
Unit I			
Chapter No. 01: Signal Representation Definition of a signals and systems, classification of signals, (analog and discrete signal, periodic and aperiodic, deterministic and random signals, even and odd signals, energy and power) , basic operation on signals(independent variable, dependent variable , time scaling, multiplication, time reversal), elementary signals (Impulse, step, ramp, sinusoidal, complex exponential), Systems Interconnections(series, parallel and cascade), properties of linear systems. (homogeneity ,superposition, linearity and time invariance, stability, memory, causality)			10
Chapter No. 02: LTI System Representation Impulse response representation and properties, Convolution, convolution sum and convolution integral. Differential and difference equation Representation, Block diagram representation			10
Unit II			
Chapter No. 03: Fourier representation for signals Introduction, Discrete time Fourier series (derivation of series excluded) and their properties. Discrete Fourier transform (derivation of transform excluded) and properties			10
Chapter No. 04: Applications of Fourier transform Introduction, frequency response of LTI systems, Fourier transform representation of periodic signals, Fourier transform representation of discrete time signals. Sampling of continuous time signals.			10
Unit III			
Chapter No. 05: Z-transform Definition of z-transform, Properties of ROC, Properties of Z-transforms: Inverse z-transforms (Partial Fraction method, long division method), Unilateral Z-transform, Transform of LTI.			10

Text Book (List of books as mentioned in the approved syllabus)

1. Simon Haykin and Barry Van Veen, Signals and Systems 2nd edition Wiley,2007
2. Alan V Oppenheim, Alan S Willsky and S. Hamid Nawab , Signals and Systems, Second, PHI public,1997

References

1. H. P Hsu, R. Ranjan, Signals and Systems, 2nd edition, McGraw Hill ,2017
2. Ganesh Raoand Satish Tunga, SignalsandSystems1st edition, Cengage India, 2017
3. M.J.Roberts, Fundamentals of Signals and Systems 2nd edition, McGraw Hill Education, 2017

Back to III Sem

III Semester Bachelor of Engineering (Electronics & Communication Engineering)		
Digital Circuits Laboratory Experiments(15EECP201)		
ISA Marks: 80	**ESA Marks: 20**	**Total Marks: 100**
Teaching Hours: 24Hrs	**Contact Hours: 2Hrs/week**	

List of Experiments:

1. Characterization of TTL Gates– Propagation delay, Fan-in, Fan-out and Noise Margin.
2. To verify of Flipflops (a) JK Master Slave (b) T-type and (c)D-Type
3. Design and implement binary to gray, gray to binary, BCD to Ex-3 and Ex-3 to BCD code converters.
4. Design and implement BCD adder and Subtractor using 4 bit parallel adder.
5. Design and implement n bit magnitude comparator using 4- bit comparators.
6. Design and implement Ring and Johnson counter using shift register.
7. Design and implement mod-6 synchronous and asynchronous counters using flip flops.
8. Design and implement given functionality using decoders and multiplexers.
9. Design and implement a digital system to display a 3 bit counter on a 7 segment display. Demonstrate the results on a general purpose PCB.

****Note-All above experiments are to be conducted along with simulation.**

Digital Circuits Lab: Simulation of combinational and sequential circuits using netlist based Spice Simulators (Avoid using drag n drop), before implementing the circuits on breadboard.

Reference Books

1. K.A.Krishnamurthy-Digital labprimer, Pearson Education Asia Publications, 2003.
2. A.P. Malvino, -Electronic Principles 7th edition, McGraw Hill Education,2017

Back to III Sem

III Semester Bachelor of Engineering (Electronics & Communication Engineering)		
Analog Electronics Laboratory Experiments(15EECP202)		
ISA Marks: 80	**ESA Marks: 20**	**Total Marks: 100**
Teaching Hours: 24Hrs	**Contact Hours: 2Hrs/week**	

List of Experiments:

Exercise

1. Design &Testing of Diode Clipping (single/double ended) circuits
2. Design &Testing of Clamping circuits for Positive and Negative Clamping.
3. Design &Testing of BJT as a switch
4. MOSFET characteristics
5. Design &Testing of MOSFET as a switch
6. Design and testing Current mirror circuit with MOSFET
7. Design and testing of Transformer-less push-pull class B power amplifier

Structured Enquiry

1. Design and study of single stage Common Emitter BJT amplifier.

A) Design and study of CS Amplifier using MOSFET.

B) Voltage series feedback

Open Ended

1. Design a regulated power supply for the given specifications.

****Note-All above experiments are to be conducted along with simulation.**

***Analog Electronic Circuits Lab:** Simulation of MOSFET based circuits using netlist based Spice Simulators (Avoid using drag n drop), with the spice models of MOSFETs in the same netlist file before using hardware using bread board.

Reference Books

1. "Electronic Devices & circuit Theory — by Nashelsky & Boylstead,11th Edition, Pearson, 2015
2. "Integrated Electronics"–By Jacob Millman and Christos Halkias ,McGraw Hill Education; 2nd edition 2017
3. "Electronic Principles" by A.P. Malvino,7th edition, McGraw Hill Education,2017

Back to III Sem

Program: III Semester Bachelor of Engineering (Electronics & Communication Engineering)		
Laboratory Experiments		
Laboratory Title: Microcontroller Architecture & Programming		Lab. Code: 15EECF202
ISA Marks: 80	ESA Marks: 20	Total Marks: 100
Teaching Hours: 52 Hrs	Contact Hours: 4 Hrs/week	Credits: 0-0-2

List of Experiments:

1. Write an 8051 ALP to verify data transfer, Arithmetic &Logical instructions.
2. Develop an 8051 ALP to perform code conversions.
3. Develop an ALP to sort an array for a given order.
4. Develop an ALP to generate prime numbers.
5. Write an 8051 C program to toggle all the bits of P0 and P2 Continuously with a 250msdelay
6. Write an ALP to generate prime numbers using subroutines.
7. Write 8051 C-program to monitor bit P1.5. If it is HIGH send 55 to P0 otherwise send AA to P2 use directives to write the program.
8. Write a program to generate a pulse train of 2seconds period on pin P2.4. Use timer1(T1) in Mode-1
9. Write a program to generate Sine wave of frequency 1KHz on pinP1
10. A square wave is being generated at pin P1.2. This square wave is to be sent to a receiver connected in serial form to 8051. Write a program to perform this operation.
11. Write a program to send a text string-Hell toserial#1. Set the baudrate at 9600,8-bit data and1-stopbit.
12. Write a C-program using interrupts to generate a 10KHz frequency on pin P2.1 usingT0.
13. Write a C'program& demonstrate an interfacing of LEDs to8051.
14. Write a C'program& demonstrate an interfacing of Switches (Momentary type, Toggle type) to8051.
15. Write a C'program& demonstrate an interfacing of Seven Segment Display: (Normal mode, BCD mode, Internal Multiplexing & External Multiplexing) to8051.
16. Write a C'program&demonstrateaninterfacingofAlphanumericLCDpanel&hexkeyboardto8051Microcontroller.
17. Write a _C'program& demonstrate an interfacing of stepper motor and DC Motor to 8051Microcontroller.
18. Build an 8051 microcontroller based application incorporating the digital circuits and should include at least two concepts of 8051 mentioned below
    1. Timers/counters
    2. Serial communication
    3. Interrupts

Books/References:

1. "The 8051 Microcontroller Architecture, Programming & Applications " By _KennethJ.Ayala, Cenage Learning; 3rd edition 2007
2. The 8051 Microcontroller and Embeddedsystems",by 'Muhammad Ali MazidiandJaniceGillespie Mazidi', 2nd edition, Pearson, 2007

Back to III Sem

Program: IV Semester Bachelor of Engineering (Electronics & Communication Engineering)			Teaching Hours
Course Title: Linear Algebra and Partial Differential Equations		Course Code: 17EMAB208	
L-T-P-SS: 4-0-0-0	Credits: 4	Contact Hours: 4Hrs/week	
ISA Marks: 50	ESA Marks: 50	Total Marks: 100	
Teaching Hours: 50Hrs	Examination Duration: 3 Hrs		
Unit I			
Chapter1: Partial differential equations Introduction, classification of PDE, Formation of PDE, Solution of equation of the type Pp + Qq = R, Solution of partial differential equation by direct integration methods, method of separation of variables. Modeling: Vibration of string-wave equation, heat equation. Laplace equation. Solution by method of separation of variables.			10
Chapter2: Finite difference method Finite difference approximations to derivatives, finite difference solution of parabolic PDE, explicit and implicit methods; Hyperbolic PDE-explicit method, Elliptic PDE-initial-boundary Value problems..			10
Unit II			
Chapter3: Fourier Series Complex Sinusoids, Fourier series representations of four classes of signals, Periodic Signals: Fourier Series representations, Derivation of Complex Co-efficient of Exponential Fourier Series and Examples. Convergence of Fourier Series. Amplitude and phase spectra of a periodic signal. Properties of Fourier Series(with proof): Linearity, Symmetry Properties, Time shift, Frequency Shift, Scaling, Time differential differentiation coefficients, Time domain Convolution, Multiplication Theorem, Parseval's theorem and Examples on these properties.			10
Chapter 4: Fourier Transform Fourier representation of non-periodic signals, Magnitude and phase spectra. Properties of Fourier Transform: Linearity, Symmetry Properties, Time shift, Frequency Shift, Scaling, Time differential differentiation coefficients, Time domain Convolution, Multiplication Theorem, Parseval's theorem and Examples on these properties.			10
Unit III			
Chapter5: Complex analysis Function of complex variables. Limits, continuity and differentiability. Analytic functions, C-R equations in Cartesian and polar forms, construction of Analytic functions (Cartesian and polar forms).			05
Chapter 7: Complex Integration Line integral, Cauchy's theorem- corollaries, Cauchy's integral formula. Taylor's and Laurent Series, Singularities, Poles, Residue theorem – problems.			05

Text Book

1. Simon Haykin, Barry Van Veen, Signals and Systems,2nd edition, Wiley,2007
2. Peter V. O'neil, Advanced Engineering Mathematics Cengage Learning Custom Publishing; 7th Revised edition2011
3. Dennis G Zilland Michae l R Cullin," Advanced Engineering Mathematics",4th edition, Narosa Publishing House, New Delhi,2012

References

1. Kreyszig E., Advanced Engineering Mathematics,10th edition,Wiley,2015
2. Stanley J Farlow, Partial differential equations for Scientists and Engineers, Dover publications, INC, New York,1993

Back to IV Sem

Program: IV Semester Bachelor of Engineering (Electronics & Communication Engineering)			Teaching Hours
Course Title: Electromagnetic Fields and Waves		Course Code: 18EECC209	
L-T-P: 3-0-0	Credits: 3	Contact Hours: 3 Hrs/week	
ISA Marks: 40	ESA Marks: 50	Total Marks: 100	
Teaching Hours: 50Hrs	Examination Duration: 3 Hrs		
Content			**Hrs**
Unit – 1			
Chapter No. 1. Introduction to Electromagnetic (EM) Waves Study of Maxwell's equations, applications of EM waves. Basic quantities and laws of electromagnetic, Maxwell's Equations, modified Ampere's law surface charge and surface current, boundary conditions at media interface			**08**
Chapter No. 2. Uniform Plane Wave Homogeneous unbound medium, wave equation for time harmonic fields, solution of the wave equation, uniform plane wave			**07**
Unit - 2			
Chapter No. 3. Uniform Plane Wave Propagation Wave Polarization, wave propagation in conducting medium, skin depth, phase velocity of a wave, power flow & pointing vector, surface current & power loss in a conductor			**08**
Chapter No. 4. Plane Waves at Media Interface Plane wave in arbitrary direction, plane wave at dielectric interface, reflection and refraction of waves at dielectric interface, normal and oblique incidence of plane waves, Brewster's Angle			**07**
Unit - 3			
Chapter No. 5. Radio Wave Propagation Modes of propagation, surface wave propagation, space wave of Ionospheric propagation, structure of troposphere and ionosphere, characteristic of Ionospheric layers, wave bending mechanism, sky wave propagation, critical frequency, virtual height, MUF, skip distance, duct propagation, fading, multi-hop propagation.			**10**

Text Book (List of books as mentioned in the approved syllabus)

1. William Hayt. Jr. John A. Buck, Engineering Electromagnetics ,9th edition, McGraw Hill Education,2018.
2. John D. Kraus, Ronald J. M.and Ahmad S. Khan, Antennas and Wave Propagation McGraw Hill Education, Fifth edition, 2017

References

1. EdwardC.JordanandKeithGBalmain,-ElectromagneticWavesAndRadiating Systems, Pearson Education, Second edition,2015
2. R. K. Shevgaonkar, Electromagnetic Waves McGraw Hill Education; 1st edition,2017
3. Mathew N. O. Sadiku, Elements of Electromagenics; Sixth edition, Oxford University, 2015
4. David J. Griffiths, Introduction to Electrodynamics Pearson Education,4th edition,2015

5. J A Edminister, Electromagnetics, , 2nd edition, McGraw Hill ,2017
6. DavidKCheng,-FieldandWaveElectromagnetics Pearson Education India; 2 edition 2014
7. John Krauss and Daniel A. Fleisch,-Electromagnetics with Applications 5th edition, McGraw Hill Education,2017
8. K.D.Prasad,-Antenna & Wave Propagation, Satyaprakash Publications,2009

Back to IV Sem

Program: IV Semester Bachelor of Engineering (Electronics & Communication Engineering)			Teaching Hours
Course Title: Linear Integrated circuits		Course Code:19EECC203	
L-T-P: 4-0-0	Credits: 4	Contact Hours: 4Hrs/week	
ISA Marks: 50	ESA Marks: 50	Total Marks: 100	
Teaching Hours: 50Hrs	Examination Duration: 3 Hrs		
Unit I			
Chapter No 1. Current Mirrors Current Mirror circuits, Current source and current sink, Figures of merit (output impedance, voltage swing), Widlar, Cascode and Wilson current Mirrors.			**4**
Chapter No 2. . Basic OPAMP architecture Basic differential amplifier, Common mode and difference mode gain, CMRR, 5-pack differential amplifier with design, 7-pack operational amplifier, Slew rate limitation, Bandwidth and frequency response curve.			**6**
Chapter No 3. OPAMP characteristics Ideal and non-ideal OPAMP terminal characteristics, Input and output impedance, output Offset voltage, Small signal and Large signal bandwidth.			**8**
Unit II			
Chapter No 4. OPAMP with Feedback OPAMP under Positive and Negative feedback, Impact Negative feedback on Bandwidth, Input and Output impedances, Offset voltage under negative feedback, Follower property & Inversion Property under linear mode operation			**10**
Chapter No 5. Linear applications of OPAMP DC and AC Amplifier, Summing, Scaling and Averaging amplifiers (Inverting, Non-inverting and Differential configuration), Instrumentation amplifier, Integrator, Differentiator, Active Filters –First and second order Low pass & High pass filters. V to I and I to V converters.			**12**
Unit III			
Chapter No 6. Nonlinear applications of OPAMP Crossing detectors (ZCD. Comparator), Inverting Schmitt trigger circuits, Triangular/rectangular wave generators, Waveform generator, Voltage controlled Oscillator, Sample and Hold circuits, Phase Shift Oscillator, Wein Bridge Oscillator, Data Converters: Digital to Analog Converters: Weighted resistor R - 2R DAC, Current steering DAC, Pipeline DAC, Analog to Digital Converters: Flash, Pipeline ADC, SAR			**10**

Text Book

1. BehzadRazavi, Fundamentals of Microelectronics 2nd edition, Wiley, 2013
2. Phillip E. Allen, Douglas R. Holberg, CMOS Analog Circuit Design 3rd edition , OUP USA ,2012
3. Ramakant A. Gayakwad, Op - Amps and Linear Integrated Circuits,. Pearson Education,4thedition, 2015

References

1. A.S. Sedra& K.C. Smith, MicroelectronicCircuits,7th edition, Oxford University Press 2017
2. Sergio Franco, Design with Operational Amplifiers and Analog Integrated Circuits, , 3rd edition , MHE ,2012
3. David A. Bell, Operational Amplifiers and LinearIC's.; Third edition, Oxford University Press, 2011
4. B. Razavi, Design of Analog CMOS Integrated Circuits, Second edition, McGraw Hill Education; 2017

Back to IV Sem

Program: IV Semester Bachelor of Engineering (Electronics & Communication Engineering)			Teaching Hours
Course Title: Control Systems		Course Code: 15EECC206	
L-T-P: 4-0-0	Credits: 4	Contact Hours: 4Hrs/week	
ISA Marks: 50	ESA Marks: 50	Total Marks: 100	
Teaching Hours: 50Hrs	Examination Duration: 3 Hrs		
Unit I			
Chapter No. 1. Control System Representation Concepts of Control Systems- Open Loop And Closed Loop Control Systems, Feed-Back characteristics, Examples, System representation: Differential Equations, Transfer function, Impulse response, System Modeling: Electrical Mechanical, Electro mechanical, Rotational Mechanical Systems.			**6**
Chapter No. 2. Block Diagram And Signal Flow Graphs Transfer Functions, Block Diagram Algebra and Representation by Signal Flow Graph - Reduction Using Mason's Gain Formula.			**8**
Chapter No. 3. Time Response Analysis Standard Test Signals (impulse, step, ramp, parabola)-Order and Type of System, Concept of Dominant pole, Time Response of First Order Systems – Characteristic Equation of Feedback Control Systems, Transient Response of Second Order Systems - Time Domain Specifications – Steady State Response - Steady State Errors and Error Constants – Effects Of Proportional Derivative, Proportional Integral Systems			**6**
Unit II			
Chapter No. 4. Stability Analysis In S-Domain The Concept Of Stability (BIBO, all system poles on LHS, Impulse response is convergent, Marginal stability- necessary conditions) – Routh's Stability Criterion – Limitations of Routh's Stability Criterion (Applications only).Root Locus Technique: The Root Locus Concept - Construction Of Root Loci.			**10**
Chapter No. 5. Frequency Response Analysis Introduction, Bode Diagrams-Determination Of Frequency Domain Specifications And Transfer Function From The Bode Diagram-Phase Margin And Gain Margin-Stability Analysis From Bode Plots, All Pass And Minimum Phase Systems			**10**
Unit III			
Chapter No. 6. Stability Analysis In Frequency Domain Polar Plots, Nyquist Plots Stability Analysis, Assessment Of Relative Stability Using Nyquist Criterion.			**6**
Chapter No. 7. Introduction to Controller Design The Design Problem. Preliminary Consideration Of Classical Design, Realization Of Basic Compensators (Lag, Lead and dominant pole compensation), P, I, PI, PD & PID Controllers.			**6**

Text Books

1. J. Nagrath and M. Gopal, Control Systems Engineering; Sixth edition, New Age International Pvt Ltd 2018
2. B. C. Kuo , Automatic Control Systems, 9th edition, John wiley and Sons,2014

References

1. Katsuhiko Ogata, Modern Control Engineering, 5th edition, Pearson education India Pvt. Ltd,2015,
2. Richord C Dorf and Robert H. Bishop, Modern Control Systems, 13th edition, Pearson; 2016

Back to IV Sem

Program: IV Semester Bachelor of Engineering (Electronics & Communication Engineering)			Teaching Hours
Course Title: ARM Processor & Applications		Course Code: 15EECC207	
L-T-P: 3-0-0	Credits: 3	Contact Hours: 3Hrs/week	
ISA Marks: 50	ESA Marks: - 50	Total Marks: 100	
Teaching Hours: 40Hrs	Examination Duration: 3 Hrs		

Content	
Unit I **Chapter 1: Introduction to Microprocessor and Microcontroller** Microprocessor, Microcontroller, Comparing Microprocessor and Microcontroller, RISC vs. CISC, Von-Neumann vs. Harvard Architecture, Microcontroller Survey, Development systems for microcontroller, Case study: Architecture of 8085/8086 and 8051 Microprocessor and Microcontroller respectively	10
Chapter 2: ARM Architecture Architectural inheritance, Architecture of ARM7TDMI, ARM programmers model, ARM development tools, 3 stage pipeline ARM organization, ARM instruction execution.	06
Chapter 3: Instruction set 1 Introduction, ARM instruction set-Data processing and branch instructions, Arithmetic and example programs Data processing instruction, Branch instruction, Load store instruction, Software interrupt instruction, Program status register instruction, Conditional execution, Example programs	06
Unit II **Chapter 4: Instruction set 2** The Thumb programmer model, Thumb branch instructions, Thumb software interrupt instructions, Thumb data processing instructions, Thumb breakpoint instruction, Thumb implementation, and Thumb applications. Example programs: The Thumb programmer model, ARM-Thumb interworking, other branch instructions, Data processing instructions, Single/Multiple register load store instruction, Stack operation, Software interrupt instructions, Thumb breakpoint instruction, Thumb implementation, and Thumb applications example programs.	05
Chapter 5: Assembler rules and Directives Introduction, structure of assembly language modules, Predefined register names, frequently used directives, Macros, Miscellaneous assembler features.	03
Chapter 6: Exception handling Introduction, Interrupts, error conditions, processor exception sequence, the vector table, Exception handlers, Exception priorities, Procedures for handling exceptions.	05
Chapter 7: Architectural support for high level languages Abstraction in software design, data types, floating point data types, The ARM floating point	

architecture, use of memory, run time environment	05
Unit – III **Chapter 8: LPC 2129/2148 Controller Architectural overview** On-chip memory, GPIOs, Timers,UART, ADC, I2C, SPI , RTC ARM interfacing techniques and programming: LED, LCD, Stepper Motor, Buzzer, Keypad,ADC	10

Text Book:

1. The 8051 Microcontroller Architecture, Programming & Applications " By KennethJ.Ayala, Cenage Learning; 3rd edition 2007
2. ARM System- on-Chip Architecture by' SteveFurber', SecondEdition,Pearson,2015
3. ARM Assembly Language fundamentals and Techniques byWilliam Hohl,CRC press CRC Press; 2nd edition,2014

References:

1. -ARM system Developer'sGuide -

Back to IV Sem

Program: IV Semester Bachelor of Engineering (Electronics & Communication Engineering)				Lab+ Teaching Hours
Course Title: Digital System Design using Verilog			Course Code: 15EECC208	
L-T-P: 0-0-2	Credits: 2		Contact Hours: 4Hrs/week	
ISA Marks: 80	ESA Marks:20		Total Marks: 100	
Teaching + Lab. Hours: 48 Hrs	Examination Duration:3 Hrs			
1.	**Introduction to verilog:** Verilog as hdl, levels of design description, simulation and synthesis, digital design flow.			02+02
2.	**Programming on Data flow description:** Structure of data-flow description, data type – vectors. Simple combinational circuit design like decoder, multiplexers, code converters.			02+02
3.	**Programming on Behavioral Descriptions:** Behavioral Description highlights, sequential statements. Introduction to Test bench. Design of sequence multiplier, Booth multiplier. Introduction to FPGAs, Synthesis			04+04
4.	**Programming on Structural Descriptions:** Highlights of structural Description, Organization of the structural Descriptions, state Machines, Generate, Generic, statements. Design of 16 bit RCA and CLA			02+02
5.	**Programming on Tasks and Functions:** Highlights of Tasks, and Functions, FSM, design like counter, Mealy and Moore machine, Sequence Detector.			04+04
6.	**Programming on Interfacing:** Interfacing with 7-segment display and push buttons. Interfacing with PS/2 Keyboard and VGA display.			04+04
7.	**Programming on Advanced HDL Descriptions:** Block RAMs on an FPGA and understand memory interfacing, File operations in Verilog, File processing examples.			02+04
8.	**Open ended Experiment:** Bowling Score Keeper / Floating Point Unit Arithmetic Units/pipelined processor/traffic light controller			06

Text Book

1. Nazeih M. Botros, HDL Programming –Verilog, Dreamtech Press,2006.
2. J.Bhaskar,-AVerilog Primer“,; 3rd edition, Pearson Education India ,2015

References

1. SamirPalnitkar,-Verilog HDL||,PearsonEducation,2ndEdition,2003.
2. Thomas andMoorby,-TheVerilogHardwareDescriptionLanguage||,kluweracademic publishers,5thedition, 2002.
3. Stephen Brown and Zvonko Vranesic,-Fundamentals ofLogicDesign with Verilog; 2nd edition, McGraw Hill Education 2017.
4. Charles.H.Roth,Jr.,Lizy Kurian John-Digital System Design using VHDL ,Thomson, 2ndEdition,2008.

Back to IV Sem

Program: IV Semester Bachelor of Engineering (Electronics & Communication Engineering)		
Course Title: Data Acquisition and Control Lab		Course Code: 15EECP203
L-T-P: 0-0-1	Credits: 1	Contact Hours: 2Hrs/week
ISA Marks: 80	ESA Marks: - 20	Total Marks: 100
Teaching Hours: 28 Hrs	Examination Duration: 2 Hrs	

List of Experiments:

1.Basic Signal Conditioning Techniques

a) Inverting and Non Inverting Amplifier using OPAMP.

b) Comparator. (ZCD &Schmitt trigger)

c) Precision rectifier

2. Realize and verify the performance of Instrumentation Amplifier using op-amp

3. Feedback Concepts: Realize and verify the performance of Wein Bridge Oscillator using op-amp

4. To design and implement the filters for a given specification

Obtain the phase and frequency responses of 2nd order, Low pass and High pass filter.

5. To implement and characterize the functional block of ADC and DAC.

Realize the following data converters to determine their respective performance parameters.

- 4-bit R-2R D-A Converter.
- 2-Bit flash ADC/4-Bit ADC (Using0804IC

6. System Modeling

- Realize the system modeling for DC Motor using Quanser Qube

7. To determine System Response of RLC circuits

Time domain response of an RLC network and the response parameters of interest (Rise time, Peak overshoot, Overshoot and Settling time) for critical, over and under damped conditions using Lab view.

Time response using Quanser Qube

8. Stability Analysis

To determine the stability of the system depending upon Pole - Zero location.

To determine the stability of the system using Bode Plots.

9. Compensation Techniques

To determine suitable compensator for the given system (PD, PI, PID Controller using Quanser Qube).

10. Structured Enquiry (16+16=32marks)

- MOS Amplifier Design and implementation

- Design and implement a PD control system using Co-simulation.

Text Books:

1. Ramakant Gayakwad, Operational Amplifiers and Linear Integrated Circuits;Fourth edition Pearson Education, 2015
2. Sergio Franco Design with Op-amps and Analog Integrated circuits,MHE; third edition,2012

References:

1. Dan Sheingold Analog to Digital Conversion Hand Book, 3rd Revised edition PH,1986. Prentice Hall,1985
2. David A. Bell, Operational Amplifiers and LinearIC's.; Third edition, Oxford University Press, 2011
3. Sedra and Smith — Microelectronics Circuits, Sixth edition, Oxford University, 2013

Back to IV Sem

Program: IV Semester Bachelor of Engineering (Electronics & Communication Engineering)		
ARM Microcontroller Laboratory Experiments(15EECP204)		
ISA Marks: 80	ESA Marks: - 20	Total Marks: 100
Teaching Hours: 28Hrs	Examination Duration: 2 Hrs	Contact Hours: 2Hrs/week

List of Experiments:

1. Writeaprogramthatdisplaysavalueof_Y'atport0and_N'atport2andalsogeneratesasquarewaveof 10Khz with Timer 0 in mode 2 at port pin p1.2 XTAL=22MHz
2. Write a C program that continuously gets a single bit of data from P1.7 and sends it to P1.0 in main, while simultaneously creating a square wave of 200us period on pin P2.5. ii. Sending letter A' to serial port. Use Timer 0to create square wave..
3. Write an ALP to achieve the following arithmetic operations: i. 32 bit addition ii. 64 bit addition iii. Subtraction iv. Multiplication v. 32 bit binary divide
4. Write an ALP for the following using loops: i. Find the sum of N' 16 bit numbers ii. Find the maximum/minimum of N numbers iii. Find the factorial of a given number with and without look up table.
5. Write an ALP to i. Find the length of the carriage r1eturn terminated string. ii. Compare two strings for equality
6. Write an ALP to pass parameters to a subroutine to find the factorial of a number or prime number generation
7. Write a _ C' program to test working of LED's usingLPC2148.
8. Write a _ C' program& demonstrate an interfacing of Alphanumeric LCD 2X16 panel to LPC2148 Microcontroller.
9. WriteanALPtogeneratethefollowingwaveformsofdifferentfrequenciesi.Squarewaveii. Triangular

a. iii. Sine wave

10. Write a _C' program & demonstrate interfacing of buzzer to LPC2148(using external interrupt)
11. Write a program to set up communication between 2 microcontrollers usingI2C.
12. Write a _C' program & demonstrate an interfacing of ADC
13. Develop an ARM based application using i. sensors ii. actuators iii. Displays

Text Books

1. Steve Furber, ARM System- on-Chip Architecture, 2nd, LPE,2002
2. The 8051 Microcontroller Architecture, Programming & Applications " By KennethJ.Ayala, Cenage Learning; 3rd edition 2007
3. William HohlARM Assembly Language fundamentals and Technique by, CRC press CRC Press; 2nd edition ,2014

Reference Books

1. -ARM systemDeveloper'sGuid- Hardbound,Publicationdate: 2004Imprint: MORGANKAUFFMAN
2. User manual onLPC21XX.

Back to IV Sem

Program: IV Semester Bachelor of Engineering (Electronics & Communication Engineering)			Lab+ Teaching Hours
Course Title: Data Structures Application Lab		Course Code: 19EECF201	
L-T-P: 0-0-2	Credits: 2	Contact Hours: 4Hrs/week	
ISA Marks: 80	ESA Marks:20	Total Marks: 100	
Teaching + Lab. Hours: 48 Hrs	Examination Duration:2 Hrs		
1.	**Hashing** Hash, Hash function, Hash Table, Collision resolution techniques, Hashing Applications		12Hrs
2.	**Trees** Computer representation, Tree properties, Binary Tree properties, Binary search trees properties and implementation, Tree traversals, AVL tree, 2-3 Tree		20Hrs
3.	**Graphs** Computer representation, Adjacency List, Adjacency Matrix, Graph properties, Graph traversals		16Hrs

Back to IV Sem

Program: V Semester Bachelor of Engineering(Electronics & Communication Engineering)			Teaching Hours
Course Title: CMOS VLSI Circuits		Course Code: 19EECC301	
L-T-P: 4-0-0	Credits: 04	Contact Hours: 6 Hrs/week	
ISA Marks: 50	ESA Marks: 50	Total Marks: 100	
Teaching Hours: 72 Hrs	Examination Duration: 3 Hrs		

Content	
Unit I **Chapter No. 1. Introduction to VLSI and IC fabrication technology** VLSI Design Flow, Semiconductor Technology - An Overview, Czochralski method of growing Silicon, Introduction to Unit Processes (Oxidation, Diffusion, Deposition, Ion-implantation), Basic CMOS technology - Silicon gate process, n-Well process, p-Well process, Twin-tub Process, Oxide isolation. FinFET device, The root cause of short channel effects in twenty-first century MOSFETS, The thin body MOSFET concept, The FinFET and a new scaling path for MOSFETs, Ultra-thin body FET, Recent trends in fabrication technology.	08
Chapter No. 2. Electronic Analysis of CMOS logic gates DC transfer characteristics of CMOS inverter, Beta Ratio Effects, Noise Margin, MOS capacitance models. Transient Analysis of CMOS Inverter, NAND, NOR and Complex Logic Gates, Gate Design for Transient Performance, Switch-level RC Delay Models, Delay Estimation, Elmore Delay Model, Power Dissipation of CMOS Inverter, Transmission Gates & Pass Transistors, Tristate Inverter.	14
Unit II **Chapter No. 3. Design of CMOS logic gates** Stick Diagrams, Euler Path, Layout design rules, DRC, Circuit extraction, Latch up – Triggering Prevention.	06
Chapter No. 4. Designing Combinational Logic Networks Gate Delays, Driving Large Capacitive Loads, Delay Minimization in an Inverter Cascade, Logical effort. Pseudo nMOS, Clocked CMOS, Dynamic CMOS Logic Circuits, Dual-rail Logic Networks: CVSL, CPL.	14
Unit – III **Chapter No. 5. Sequential CMOS Circuit Design** Sequencing static circuits, Circuit design of latches and flip-flops, Clocking- clock generation, clock distribution.	08

Text Books (List of books as mentioned in the approved syllabus)

1. John P.Uyemura, Introduction to VLSI Circuits and Systems, 1, Wiley, 2007
2. Neil Weste, David Harris &AyanBanerjee,CMOS VLSI Design, 4, Pearson Ed 2011
3. Sung-Mo Kang & Yusuf Leblebici, CMOS Digital Integrated Circuits: Analysis and Design, 3, Tata McGra, 2007

References

1. FinFET Modeling for IC Simulation and Design: Using the BSIM-CMG Standard By Yogesh Singh Chauhan, Darsen Duane Lu, VanugopalanSriramkumar, SourabhKhandelwal, Juan Pablo Duarte, NavidPayvadosi, Ai Niknejad, Chenming Hu, Elsevier Publication, 2015
2. Wayne, Wolf, Modern VLSI design: System on Silicon, 3, Pearson Ed,2005
3. Douglas A Pucknell and Kamran Eshraghian, Basic VLSI Design, 3rd edition, PHI,2005
4. Phillip. E. Allen, Douglas R. Holberg, CMOS Analog circuit Design, 3rd edition, Oxford University,2011

Back to V Sem

Program: V Semester Bachelor of Engineering (Electronics & Communication Engineering)			Teaching Hours
Course Title: Communication Systems I		Course Code: 21EECC302	
L-T-P: 4-0-0	Credits: 4	Contact Hours: 4 Hrs/week	
ISA Marks: 50	ESA Marks: 50	Total Marks: 100	
Teaching Hours: 50Hrs	Examination Duration: 3 Hrs		

Content	
Unit – 1	**Hours**
Chapter 01. Analog Communication Techniques: Introduction, need for modulation, Amplitude modulation, Time-Domain description, Frequency-Domain description. Generation of AM wave- square law modulator. Detection of AM waves, square law and envelope detector. Double side band suppressed carrier modulation (DSBSC), Generation of DSBSC waves: balanced modulator. Coherent detection of DSBSC modulated waves: Costas loop. Quadrature carrier multiplexing. Single side band modulation, Frequency-Domain and time-domain description of SSB modulated Signals-Generation, detection. Comparison of amplitude modulation techniques, Frequency division multiplexing (FDM).	**14 Hours**
Chapter 02. Receiver and its characteristics: Radio receivers: Tuned radio frequency receiver, Super heterodyne receiver Sensitivity and selectivity, selection of IF. Block diagram and features of Communication Receiver.	**06 Hours**
Unit – 2	
Chapter 03. Angle modulation: Basic definitions, Phase and frequency modulation, Phase and frequency Deviation, Narrow and Wide band frequency modulation. Spectrum and phase diagram of FM Transmission band width of FM waves, Effect of Modulation index on bandwidth, Generation of FM Waves: indirect FM, Direct FM, Demodulation of FM Waves,	**08 Hours**
Chapter 04. Random Variables and processes: Random variables-average, variance, CDF, PDF, Joint CDF and PDF, Random Process- Stationary, Mean, Correlation and Covariance functions., autocorrelation function, Cross-correlation functions. Power spectral density: Properties of the spectral density, Gaussian Process: Central limit theorem, Properties of Gaussian processes.	**06 Hours**
Chapter 05. Noise in Continuous wave modulation Systems: Sources of noise: Shot noise, thermal noise, White noise. Frequency domain representation, Effect of filtering on Gaussian noise, Mixing and superposition of Noises, Noise equivalent bandwidth, Quadrature components of noise, Narrowband noise, Noise figure., Equivalent noise temperature. Receiver model, Noise in AM Receivers, Noise in FM receivers	**06 Hours**
Unit - 3	
Chapter 06. Introduction to Sampling: Sampling theorem, Quadrature sampling of Band pass signals, Reconstruction of a message from its samples. Time Division Multiplexing (TDM) Signal distortion in Sampling.	**10 Hours**

Text book:

1. "Communication Systems" by 'Simon Haykin' John Wiley 2003. 5th edition , 2009
2. "Principles of communication Systems", by Taub & Schilling, 2nd edition , TMH.
3. "Digital communications", Simon Haykin, John Wiley, 2006

References

1. Communication Systems, by B.P.Lathi ,
2. Ganesh Rao, K N Haribhat, Analog Communication, Sanguine, 2009
3. Communication Systems by Harold. P.E, Stern Samy. A. Mahmond, Pearson Education, 2004.
4. Electronic communication systems, Kennedy and Davis, TMH, Edn. 6, 2012

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Back to V Sem

Program: V Semester Bachelor of Engineering (Electronics & Communication Engineering)			Teaching Hours
Course Title: Digital Signal Processing		Course Code: 17EECC303	
L-T-P: 4-0-0	Credits: 4	Contact Hours: 4Hrs/week	
ISA Marks: 50	ESA Marks: 50	Total Marks: 100	
Teaching Hours: 50Hrs	Examination Duration: 3 Hrs		
Content			
Unit – 1			
Chapter No. 1. Discrete Fourier Transforms Brief review of signals and systems: Basic definitions, properties and applications. Discrete Fourier Transforms (DFT): Frequency domain sampling and reconstruction of discrete time signals. DFT as a linear transformation, its relationship with other transforms. Properties of DFT, multiplication of two DFTs- the circular convolution, additional DFT properties, use of DFT in linear filtering, overlap-save and overlap-add method.			**12**
Chapter No. 2. Fast-Fourier-Transform (FFT) algorithms Fast-Fourier-Transform (FFT) algorithms: Direct computation of DFT, Need for efficient computation of the DFT (i.e. FFT algorithms), Radix-2 FFT algorithm for the computation of DFT and IDFT: Decimation-in-time and Decimation-in-frequency algorithms, Composite FFT.			**08**
Unit – 2			
Chapter No. 3. Design of Digital FIR Filters Design of digital filters: Considerations and characteristics of practical digital filters. design of digital filters: symmetric and anti-symmetric FIR filters, design of linear phase FIR filters using windowing method- Rectangular, Hamming, Hanning, Bartlet and Kaiser windows. Design of linear phase FIR filters using frequency sampling technique.			**10**
Chapter No. 4. Design of IIR filters from analog filters Design of IIR filters from analog filters: approximation of derivative, impulse invariance method, bilinear transformation, Characteristics of commonly used analog filters: Butterworth and Chebyshev filters, frequency transformation in the digital domain.			**10**
Unit – 3			
Chapter No. 5. Realization of Digital FIR Systems Implementation of Digital systems: structures for FIR systems: direct form I, direct form II, cascade, frequency sampling and lattice structure, Comparison of the realization techniques.			**05**
Chapter No. 6. Realization of Digital IIR Systems Structures for IIR systems - direct form I, direct form II, cascade, parallel and lattice structure, Comparison of the realization techniques.			**05**

Text Books

1. Proakis & Manolakis, Digital signal processing Principles Algorithms & Applications, 4th edition, PHI, New Delhi,2007
2. S.K. Mitra, Digital Signal Processing, 2nd edition, Tata Mc-Graw Hill,2004

References

1. Oppenheim& Schaffer, Discrete Time Signal Processing, 5th edition, PHI, New Delhi, 2000

Back to V Sem

Program: V Semester Bachelor of Engineering (Electronics & Communication Engineering)			Teaching Hours
Course Title: Operating System and Embedded System Design		Course Code: 17EECC304	
L-T-P: 3-0-0	Credits: 3	Contact Hours: 3Hrs/week	
ISA Marks: 50	ESA Marks: 50	Total Marks: 100	
Teaching Hours: 40 Hrs	Examination Duration: 3 Hrs		
Unit I			
Chapter 1: Introduction and System structures what is an operating system? Goals of an operating system. Operation of an os. Resource allocation and related functions. Classes of an operating system. Operating System Services. System Calls and Types. Operating system Structure – Simple, Layered, Microkernels, Modules and Hybrid systems. System Boot			**03**
Chapter 2: Process Management Process concept- operating on process, inter process communication, process scheduling- CPU scheduler- preemptive scheduling , scheduling criteria, scheduling algorithms- first come first served scheduling, shortest job first scheduling, priority scheduling, round robin scheduling.			**05**
Chapter 3: Memory Management Memory Management Strategies: process address space static vs dynamic loading. Swapping, memory allocation; fragmentation Paging; Structure of page table; Segmentation, Virtual Memory.			**06**
Unit II			
Chapter 4: Introduction To Real-Time Operating Systems Introduction To Real-Time Operating Systems: Introduction to OS, Introduction to real time embedded system- real time systems, characteristics of real time systems and the future of embedded systems. Introduction to RTOS, key characteristics of RTOS, its kernel, components in RTOS kernel, objects, scheduler, services, context switch, Scheduling types: Preemptive priority-based scheduling, Round-robin and preemptive scheduling.			**08**
Chapter 5: Tasks, Semaphores and Message Queues: Tasks, Semaphores and Message Queues: A task, its structure, A typical finite state machine, Steps showing the how FSM works. A semaphore, its structure, binary semaphore, mutual exclusion (mutex) semaphore, Synchronization between two tasks and multiple tasks, Single shared-resource-access synchronization, Recursive shared- resource-access synchronization. A message queue, its structure, Message copying and memory use for sending and receiving messages, Sending messages in FIFO or LIFO order, broadcasting messages.			**08**
Unit III			
Chapter 6: Typical Embedded System: Classification and purposes of embedded system, Characters and Quality attributes of embedded system, Core and Supporting components of embedded system, Embedded firmware			**05**
Chapter 7: Wired and Wireless Protocols: Bus communication protocol (USB,I2C,SPI), Wireless and mobile system protocol (Bluetooth, 802.11 and its variants, ZigBee), Embedded design cycle-case study-ACVM			**05**

Text Books

1. Silberschatz ,Galvin and Gagne ,‖Operating system concepts‖,9th edition, WILEYPublication,2018.
2. Qing Li with Caroline Yao, Real-Time Concepts for Embedded Systems, 1E, Published,2011
3. Shibu K V,‖Introductionto Embedded systems‖,2nd edition, McGraw Hill Education India Private Limited,2017
4. Raj Kamal,‖ Embedded Systems‖, Paperback,3rd edition, McGraw-Hill Education, 2017

References

1. DhananjayDhamdhere,‖Operating Systems a Concept Based Approach‖,3rd edition, McGraw-HillEducation,2017

Back to V Sem

Program: V Semester Bachelor of Engineering (Electronics & Communication Engineering)			Teaching Hours
Course Title: Machine Learning		Course Code: 17EECC307	
L-T-P: 2-0-1	Credits: 3	Contact Hours: 4 Hrs/week	
ISA Marks: 50	ESA Marks: 50	Total Marks: 100	
Teaching Hours: 50Hrs	Examination Duration: 3 Hrs		

Content	
Unit – 1	Hrs
Chapter No. 1. Introduction Introduction what is machine learning? Applications of machine learning, types of machine learning: supervised, unsupervised and reinforcement learning, dataset formats, basic terminologies.	**05**
Chapter No. 2. Supervised Learning Linear regression, logistic regression linear regression: single and multiple variables, sum of squares error function, the gradient descent algorithm, application, logistic regression, the cost function, classification using logistic regression, one-v/s-all classification using logistic regression, regularization.	**10**
Unit – 2	
Chapter No. 3. Supervised Learning: Neural Network Introduction to perception learning, implementing simple gates XOR, AND, OR using neural network. Model representation, gradient checking, back propagation algorithm, multi-class classification, application- Classifying digits, SVM.	**10**
Chapter No. 4. Unsupervised Learning: Clustering Introduction, K means clustering, algorithm, cost function, application.	**05**
Unit – 3	
Chapter No. 5. Unsupervised Learning: Dimensionality reduction Dimensionality reduction, PCA- principal component analysis, applications, clustering data and PCA.	**04**

Text Book

1. Tom Mitchell, Machine Learning, 1st edition, McGraw-Hill. , 2017
2. Christopher Bishop, Pattern Recognition and Machine Learning, 1, Springer, 2nd printing 2011 edition

References

1. Video lectures by : Andrew Ng, Co-founder, Coursera; Adjunct Professor, Stanford University; formerly head of Baidu AI Group/Google Brain

   https://www.coursera.org/learn/machine-learning#

2. Trevor Hastie, Robert Tibshirani, Jerome Friedman, The Elements of Statistical Learning : Data Mining, Inference and Prediction, 2nd edition, Springer, 9th printing 2017 edition

Back to V Sem

Program: V Semester Bachelor of Engineering (Electronics & Communication Engineering)			Teaching Hours
Course Title: Communication and Signal Processing Lab		Course Code: 17EECP301	
L-T-P: 0-0-1	Credits: 1	Contact Hours:2 Hrs/week	
ISA Marks: 80	ESA Marks: 20	Total Marks: 100	
Teaching Hours: 24Hrs	Examination Duration: -		

List of Experiments

Proof of concept on Discrete ICs

1. DSBSC modulator and demodulator.
2. Frequency modulator and demodulator
3. Frequency Shift Keying (FSK) modulator and demodulator.
4. Time Division Multiplexing with minimum four channels

Mathematical Modeling and Simulation

1. Design Square Law Modulator and detect the signal using square law and envelop schemes.
2. Design Frequency Modulator and Demodulator and analyze the performance without and with noise.
3. Design, analyze and compare the BER for different digital modulation techniques.
4. Develop a model and simulate BPSK using Costa sloop.

Implementation on Real Time Hardware

1. Design and Implement a complete real-time RF transceiver on Advanced Omni Software Radio Transceiver (AOSRT) for Narrow Band Frequency Modulation and Wide band Frequency Modulation and perform analysis.
2. Design and Implement a real-time RF transceiver for audio input using M-array PSK modulation scheme and analyze performance in terms of SNR and BER.

Open Ended Experiment

1. Explore the features of SDR to design an appropriate and robust frequency selective system to eliminate noise present in an audio signal.

Back to V Sem

Program: V Semester Bachelor of Engineering (Electronics & Communication Engineering)		
CMOS VLSI Circuits Laboratory Experiments	Course Code: 19EECP301	
ISA Marks: 80	ESA Marks: 20	Total Marks: 100
Teaching Hours: 25Hrs	Examination Duration: 2 Hrs	Contact Hours: 2Hrs/week

List of Experiments:

1. Introduction to Cadence EDA tool.
2. Static and Dynamic Characteristic of CMOS inverter.
3. Layout of CMOS Inverter(DRC,LVS)
4. Static and Dynamic Characteristic of CMOS NAND2 andNOR2.
5. Layout of NAND2, NOR2, XOR2 gates (DRC,LVS).

Structured Enquiry

1.Design a Phase Detector using D-FF

Open Ended

1. Design complex combinational circuits and analyze the performance using Cadence tool.

Books/References:

1. JohnP.Uyemura,-Introduction to VLSI Circuits and System, Wiley, 2006.
2. Neil Weste and K. Eshragian Principles of CMOS VLSI Design: A System Perspective,‖ 2nd edition, Pearson Education (Asia) Ptv. Ltd.,2000.

Back to V Sem

Program: V Semester Bachelor of Engineering (Electronics & Communication Engineering)		
RTOS Laboratory Experiments		**Course Code: 17EECP302**
ISA Marks: 80	**ESA Marks: - 20**	**Total Marks: 100**
Teaching Hours: 24Hrs	**Examination Duration: -**	**Contact Hours: 2 Hrs/week**

List of Experiments:

1. Analyze and Demonstrate debugging skills for programs given.
2. Program & demonstrate interfaces I2C-memory to LPC2148Microcontroller.
3. Program & demonstrate interfaces SPI-RTC to LPC2148Microcontroller.
4. Program & demonstrate concept of H/W Interrupts interface to LPC2148Microcontroller.
5. Program & demonstrate concept of Task Scheduling.
6. Program & demonstrate concept of Semaphore.
7. Program & demonstrate concept of Mailbox.
8. Program & demonstrate concept of S/W Interrupts.
9. Program & demonstrate concept of interrupts.
10. Program & demonstrate concept of Inter Task Communication.

Reference Books

1. -ARMSystem- on-Chip Architecture By'SteveFurber,LPE,SecondEdition, Addison Wesley; 2000 .
2. -EmbeddedSystems-Architecture,ProgrammingandDesign||byRajKamal,3rd edition,TMH,2017
3. Dr.K.V.K.K.Prasad,-Embedded/Realtimesystems:concepts,Design&Programming||,publishedbydreamtechpress, 2003

Manual

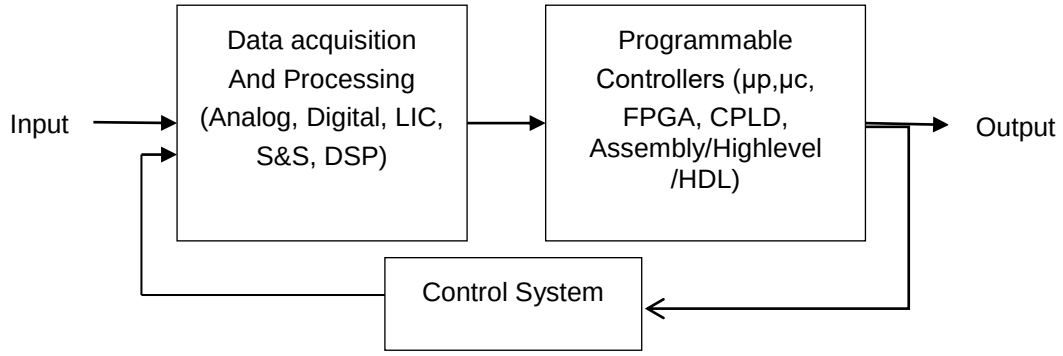
1. LPC2148 datasheet byNXP.
2. LPC2148 board manual by ALS,Bangalore.

Back to V Sem

Laboratory Title: **Mini Project**	Lab. Code: **17EECW301**
Total Hours: **60**	Duration of ESA Hours: **3 Hours**
ISA Marks: **50**	ESA Marks: **50**

Guide lines for selection of a project:

1. The project needs to encompass the concepts leant in a subject/s studied in the previous four semesters, so that the student will learn to integrate, the knowledge base acquired to provide a solution to the identified need.
2. Project should be able to exhibit sensing, controlling and actuation sections.
3. The mini project essentially will comprise of two components:
   - The hardware design
   - The graphical user interface (GUI) for application and data analysis with report generation.



4. Student can select a project which leads to a product or model or prototype related to following areas (not limited to these areas).
   - Pulse and digital circuits: simulate the working of one or more circuits
   - Signals and systems: simulate the behavior of a system by considering different signals
   - Analog Electronic: simulate working of different devices
   - Control systems: simulate the behavior of a control system
   - Linear Integrated Circuits: simulate working of one or more circuits
   - Micro-controllers: simulate the ALU/control unit of microcontroller
5. Time plan: Effort to do the project should be between 120-150 Hrs per team, which includes self study of an individual member (80-100 Hrs) and team work (40-50hrs).
6. Learning overhead should be 20-25% of total project development time.

Back to V Sem

Program: VI Semester Bachelor of Engineering (Electronics & Communication Engineering)			Teaching Hours
Course Title: Automotive Electronics		**Course Code: 17EECC305**	
L-T-P: 3-0-0	**Credits: 3**	**Contact Hours: 3Hrs/week**	
ISA Marks: 50	**ESA Marks: 50**	**Total Marks: 100**	
Teaching Hours: 40 Hrs	**Examination Duration: 3 Hrs**		
Unit I **Chapter 1: Introduction: Automotive Systems, Design cycle and Automotive industry overview :** Overview of Automotive industry, Vehicle functional domains and their requirements, automotive supply chain, global challenges. Role of technology in Automotive Electronics and interdisciplinary design.. Introduction to modern automotive systems and need for electronics in automobiles and application areas of electronic systems in modern automobiles, Introduction to power train, Automotive transmissions system ,Vehicle braking fundamentals, Steering Control, ,Overview of Hybrid Vehicles, ECU Design Cycle : Types of model development cycles (V and A) , Components of ECU, Examples of ECU on Chassis, Infotainment, Body Electronics and cluster.			**07**
Chapter 2: Embedded system in Automotive Applications & Automotive safety systems Automotive grade microcontrollers: Architectural attributes relevant to automotive applications, Automotive grade processors ex: Renesas, Quorivva, Infineon. EMS: Engine control functions, Fuel control, Electronic systems in Engines , Development of control algorithm for EMS, Look-up tables and maps, Need of maps, Procedure to generate maps, Fuel maps/tables, Ignition maps/tables, Engine calibration, Torque table, Dynamometer testing Safety Systems in Automobiles: Active and Passive safety systems: ABS, TCS, ESP, Brake assist, Airbag systems etc.			**08**
Unit II **Chapter 3: Automotive Sensors and Actuators** Sensor characteristics, Sensor response, Sensor error, Redundancy of sensors in ECUs, Avoiding redundancy, Smart Nodes , Examples of sensors : Accelerometer (knock sensors),wheel speed sensors, Engine speed sensor, Vehicle speed sensor, Throttle position sensor, Temperature sensor, Mass air flow (MAF) rate sensor, Exhaust gas oxygen concentration sensor, Throttle plate angular position sensor, Crankshaft angular position/RPM sensor, Manifold Absolute Pressure (MAP) sensor. Actuators: ENGINE CONTROL ACTUATORS, Solenoid actuator, Exhaust Gas Recirculation Actuator.			**08**
Chapter 4: Automotive communication protocols : Overview of Automotive communication protocols : CAN, LIN , Flex Ray, MOST			**07**
Unit III **Chapter 5: Advanced Driver Assistance Systems (ADAS) and Functional safety standards:** Advanced Driver Assistance Systems (ADAS): Examples of assistance applications: Lane Departure Warning, Collision Warning, Automatic Cruise Control, Pedestrian Protection, Headlights Control, Connected Cars technology and trends towards Autonomous vehicles. Functional Safety: Need for safety standard-ISO 26262, Safety concept, safety process for product life cycle, safety by design, validation.			**05**

Chapter 6: Diagnostics : Fundamentals of Diagnostics**,** Basic wiring system and Multiplex wiring system, Preliminary checks and adjustments, Self-diagnostic system. Fault finding and corrective measures, Electronic transmission checks and Diagnosis, Diagnostic procedures and sequence, On board and off board diagnostics in Automobiles, OBDII, Concept of DTCs, DLC, MIL, Freeze Frames, History memory, Diagnostic tools, Diagnostic protocols KWP2000 and UDS	**05**

Text Books

1. Ribbens, Understanding of Automotive electronics, 8th edition , Elsevier,2017
2. Denton.T , Automobile Electrical and Electronic Systems, 5th edition, Routledge, 2017
3. Denton.T , Advanced automotive fault diagnosis, 4th edition Routledge, 2016

References

1. Ronald K Jurgen, Automotive Electronics Handbook, 2nd Edition, McGraw-Hill,1999
2. James D Halderman, Automotive electricity and Electronics, 5th edition, Pearson, 2016
3. Allan Bonnick, Automotive Computer Controlled Systems Diagnostic Tools and Techniques, Elsevier Science,2001
4. Nicholas Navet , Automotive Embedded System Handbook ,2009

Back to VI Sem

Program: VI Semester Bachelor of Engineering (Electronics & Communication Engineering)			Teaching Hours
Course Title: Computer Communication Networks		Course Code: 17EECC306	
L-T-P: 4-0-0	Credits: 4	Contact Hours: 4 Hrs/week	
ISA Marks:50	ESA Marks: 50	Total Marks: 100	
Teaching Hours: 50Hrs	Examination Duration: 3 Hrs		

Content	Hrs
Unit – 1	
Chapter No. 1. Computer Networks and the Internet What is Internet? The Network Edge, the network Core,delay -loss—throughput in packet switched networks. Protocol layers (OSI layers) and their service models, networks under attack.	08 hrs
Chapter No. 2. Application Layer Principles of network applications,the web and HTTP,DHCP, file transfer-FTP, electronic mail in the internet,DNS,peer-to-peer applications, socket programming-creating network applications	12 hrs
Unit – 2	
Chapter No. 3. Transport Layer Introduction and transport-layer services-relationship between transport and network layers - overview of the transport layer in the internet, multiplexing and de multiplexing, connectionless transport: UDP, principles of reliable data transfer, connection oriented transport TCP, TCP congestion control.	10 hrs
Chapter No. 4. Network layer Introduction, virtual circuit and datagram networks, what's inside router? The Internet protocol (IP): forwarding and addressing in the internet, routing algorithms, routing in the internet, broadcast and multi cast routing.	10 hrs
Unit – 3	
Chapter No. 5. The link layer: Links, Access networks, and LANs Introduction to the link layer, error-detection and correction techniques, multiple access links and protocols, switched local area networks, link virtualization: A network as a link layer, data center networking, retrospective: A day in the life of a web page request.	10 hrs

Text Book

1. Kurose&Ross,ComputerNetworkingATop-DownApproach,6th editionPEARSON,2013.

References

1. LarryL. Peterson&BruceS.Davie,ComputerNetworks:ASystemsApproach,5th edition, Elsevier, 2011
2. Behrouz A. Forouzan, Data Communication and Networking,Paperback, 5th edition, TMG,2017

Back to VI Sem

Program: VI Semester Bachelor of Engineering (Electronics & Communication Engineering)			Teaching Hours
Course Title: Communication Systems II		Course Code: 21EECC307	
L-T-P: 3-0-0	Credits: 3	Contact Hours: 3 Hrs/week	
ISA Marks: 50	ESA Marks: 50	Total Marks: 100	
Teaching Hours: 42Hrs	Examination Duration: 3 Hrs		

Content	
Unit – I	**Hours**
Chapter 01. Quantization and Coding techniques: Quantization, PCM, quantization noise and SNR, robust quantization, DPCM, DM, ADM, coding speech at low bit rates, applications, Binary data formats	**06 Hrs**
Chapter 02. Digital Modulation Techniques: Digital Modulation formats, Coherent binary modulation techniques, Coherent quadrature modulation techniques. Non-coherent binary modulation techniques, Comparison of Binary and Quaternary Modulation techniques. M-ary Modulation Techniques, effect of ISI, Bit versus Symbol error probability, Synchronization and applications	**10 Hrs**
Unit – II	
Chapter 03. Base band shaping for data transmission: Base-Band Shaping for Data Transmission, Discrete PAM signals, power spectra of discrete PAM signals. ISI, Nyquist's criterion for distortion less base-band binary transmission, correlative coding, eye pattern, base-band M-ary PAM systems, and adaptive equalization for data transmission.	**06 Hrs**
Chapter 04. Detection and Estimation: Gram-Schmidt Orthogonalization procedure, geometric interpretation of signals, response of bank of correlators to noisy input, Detection of known signals in noise, probability of error, correlation receiver, matched filter receiver, detection of signals with unknown phase in noise, estimation: concept and criteria, maximum likelihood estimation.	**08 Hrs**
Chapter 05. Introduction to Information Theory: Basics of Information, Discrete communication channels.	**02 Hrs**
Unit - III	
Chapter 06. Information Theory: Information Theory: Introduction, Measure of information, Average information content of symbols in long independent sequences, Average information content of symbols in long dependent sequences.	**08 Hrs**

Text Book:

1. Simon Haykin, Digital communications, John Wiley, 2006
2. K. Sam Shanmugam, Digital and analog communication systems, John Wiley, 2006

Reference Book:

1. Simon Haykin, An introduction to Analog and Digital Communication, John Wiley, 2003

Back to VI Sem

Program: VI Semester Bachelor of Engineering (Electronics & Communication Engineering)		
Computer Communication Networks Laboratory Experiments(17EECP303)		
ISA Marks: 80	**ESA Marks: - 20**	**Total Marks: 100**
Teaching Hours: 24Hrs	**Examination Duration:-**	**Contact Hours: 2 Hrs/week**

List of Experiments

1. Introduction to Hardware components and Ethernet LAN setup.
2. Introduction to socket programming
3. Implementation of FTP
4. Implementation of error control techniques.
5. Implementation of flow controlARQs
6. Introduction to Network operating system.
7. Subnet design
8. VLAN setup
9. OSPF and RIP configuration and performance analysis
10. eBGP and iBGP configuration and performance analysis

Text Book.

1. Kurose&Ross, ComputerNetworkingATop-DownApproach,6theditionPEARSON, 2013.

References

1. Cisco networking academy,https://www.netacad.com/
2. Juniper networking academy,https://learningportal.juniper.net/

Back to VI Sem

Program: VI Semester Bachelor of Engineering (Electronics & Communication Engineering)		
Automotive Electronics Laboratory Experiments(17EECP304)		
ISA Marks: 80	**ESA Marks: - 20**	**Total Marks: 100**
Teaching Hours: 24Hrs	**Examination Duration:-**	**Contact Hours: 2 Hrs/week**

List of Experiments

1. Demonstration of cut section modules: Engine, Transmission, Steering, Braking, Suspension - Automobile dept.
2. Electronic engine control system: Injection and Ignition control system Transmission trainer modules
3. Modeling a vehicle motion on a flat surface during hard acceleration, deceleration and steady acceleration.
4. Simulation and modeling of a system and realization on the hardware platform.
5. Modeling Seat belt warning system, and Vehicle speed control based on the gear input.
6. EGAS modeling and simulation using Simulink and realization on the hardware platform.
7. Interior lighting control modeling with state flow.
8. Gear input transmission over CAN bus using ARM Cortex m3 and signal analysis using CANalyzer/BusMaster software.
9. Realize Steer by wire system using model based design.
10. Realize cruise application using model based design

Text Books

1. Ribbens, Understanding of Automotive electronics, 6th , Elsevier,2003
2. Denton.T , Automobile Electrical and Electronic Systems, 5th edition, Routledge, 2017

Back to VI Sem

Laboratory Title: Minor Project	*Lab. Code*: 17EECW302
Total Hours: 70	*Duration of Exam*: Hours: 2
Total Exam Marks: 50	*Total ISA. Marks*: 50

Application Areas are,

- Smart City
- Connected Cars
- Home Automation
- Health care
- Smart energy
- Agriculture

Guide lines for selection of a project:

1. The project needs to encompass the concepts leant in a subject/s studied in the previous five semesters, so that the student will learn to integrate, the knowledge base acquired to provide a solution to the defined problem statement of the minor-projects.
2. Student can select a project which leads to a product or model or prototype.
3. Time plan: Effort to do the project should be between 120-150 Hrs per team, which includes self study of an individual member (80-100 Hrs) and team work (40-50hrs).
4. Learning overhead should be 20-25% of total project development time.

Criteria for group formation :

1. 3-4 students in a team.
2. Role of teammates: Team lead and members.

Allocation of Guides and Mentors for the projects:

Every Project batch will be allocated with one faculty.

Details of the project batches:

1. Number of faculty members : 64
2. Number of students: 278

Role of a Guide

The primary responsibility of the guide is to help students to understand the meaning and need of various stages in the implementation of the project. At every stage of the project development, guide should help towards its successful completion as per the predefined standards.

How student should carry out a project:

1. Define the problem
2. Specify the requirements
3. Specify the design in the understandable form (Block Diagram, Flowchart, Algorithm,etc)
4. Analyze the design
5. Select appropriate simulation tool and development board for the design.

6. Implement the design
7. Optimize the design and generate the results with optimized design.
8. Result representation and analysis
9. Prepare a document and presentation.

Report Writing

1. The format for report writing should be downloaded from ftp://10.3.0.3/minorprojects
2. The report needs to be shown to guide and committee for each review.

Back to VI Sem

Course Title: Analog Circuit Design		Course Code: 17EECE301
L-T-P: 3-0-0	Credits: 3	Contact Hours: 3
CIE Marks: 50	SEE Marks: 50	Self-Study : --
Teaching Hours: 40	Examination Duration: 3 hours	Total Marks: 100

UNIT I	04
Basic MOS Device Physics: General considerations, MOS I/V characteristics, second order effects and MOS device models.	04
Current Mirrors: Basic current Mirror, Widlar, Cascode and Wilson Current Mirrors.	08
Single Stage Amplifiers: CS, CG, CD, Cascode and Folded Cascode. Frequency response curves	
UNIT II	
Differential Amplifiers: Differential Amplifier, 5 pack differential Amplifier, CMRR, PSRR	05
Op-Amp: Performance parameters, Two stage (7-pack) Op-amp, Slew rate, PSRR , Noise in Op-amps	05
Compensation Technique: Nyquist stability Criterion, Gain and Phase margins, Compensation of Two stage op-amp and Dominant pole compensation technique.	06
UNIT III	
Reference Circuits: Current reference, startup circuits, Bandgap reference circuit, Current mode Bandgap reference.	04
Comparators: Basic Comparator architecture, non-idealities-offset error, bandwidth consideration, Dynamic comparator,	

Text Books

1. B Razavi 'Design of Analog CMOS Integrated Circuits' First Edition McGraw Hill 2001
2. Phillip. E. Allen, Douglas R. Holberg, "CMOS Analog circuit Design" Oxford University Press, 2002.
3. Baker, Li, Boyce, "CMOS: Circuit Design, Layout and Simulation", Prentice Hall of India, 2000

Reference Books

1. N. Weste and K. Eshranghian, Principles of CMOS VLSI Design, Addison Wesley. 1985.
2. J. Rabaey, Digital Integrated Circuits: A Design Perspective, Prentice Hall India, 1997

Back to VI Sem Elective

Program: VI Semester Bachelor of Engineering (Electronics & Communication Engineering)			Teaching Hours
Course Title: Introduction to Deep Learning		Course Code: 19EECE322	
L-T-P: 2-0-1	Credits: 3	Contact Hours: 3 Hrs/week	
CIE Marks: 50	SEE Marks: 50	Total Marks: 100	
Teaching Hours: 42Hrs	Examination Duration: 3 Hrs		
Unit I **Chapter 1: Introduction to Deep Learning:** What is Deep Learning?, Applications of deep learning, Differences between machine learning and deep learning, Basics of Neural Networks, Supervised Learning with Neural Networks, Logistic regression as a neural network, Computation graph, shallow neural networks, Deep neural networks **Chapter 2: Hyper-Parameter Tuning, Regularization and Optimization:** Basics of Hyper-parameters, Regularization, Need for regularization, dropout regularization, gradient checking, mini-batch gradient descent, exponentially weighted averages and its bias correction, Gradient descent with decay, Adam's optimization algorithm, The problem of local minima, weight initialization in neural networks, Normalizing activations in a network, Fitting Batch norm into a network, Softmax regression, Softmax classifier, Introduction to metric tensors and tensorflow, Basic programs in tensorflow.			06 Hrs 10 Hrs
Unit II **Chapter 3: Convolutional Neural Networks** Introduction to Computer Vision and Image Processing, 2D Convolutions, Strided convolution, convolution over volume, One layer of a convolution network, ReLu and pooling, Example of a ConvNet, Classic CNN Networks, ResNet architecture, Inception Networks, Transfer learning, Data Augmentation, Basics of Keras, Residual networks, Object Localization, Landmark and object detection, Convolutional implementation of sliding windows, YOLO algorithm, Car detection algorithm using YOLO, One shot learning, Face recognition algorithm. **Chapter 4: Recurrent Neural Networks** Backpropogation through time, RNN model, Types of RNN, Vanishing gradients with RNN, Gated Recurrent Unit, LSTM, Bidirectional RNN, Deep RNN, basics of NLP and Concept of word embedding, speech recognition.			12 Hrs 04 Hrs
Unit III **Chapter 5: Unsupervised Deep Learning** Concepts of Unsupervised deep learning, RBM (Restricted Boltzman Machine) and auto encoders, structure of Auto encoders, collaborative filtering with RBM, Deep belief networks.			10 Hrs

Text Books

1. Deep Learning, Ian Good fellow and Yoshua Bengio and Aaron Courville, MIT Press, http://www.deeplearningbook.org, 2016.
2. *Neural Networks and Deep Learning* by Michael Nielsen.

References

3. Deep Learning with Python, Francois Chollet, by Manning Publications, 2018.
4. Deep Learning by Microsoft Research
5. Deep Learning Tutorial by LISA lab, University of Montreal

Back to VI Sem Elective

Course Code: 15EHSA401	Course Title: CIPE & EVS	
L-T-P : Audit	Credits: Audit	Contact Hrs: 32
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hrs: 32		Exam Duration: 3 hours

Content	Hrs
Unit – 1	
Chapter No. 1 Features of Indian Constitution Features of Indian Constitution, Preamble to the constitution of India, Fundamental rights under Part III – details of Exercise of rights, Limitations & Important cases. Berubari Union and Exchange of Enclaves, Kesavan and Bharati vs. UOI, Maneka Gandhi vs. UOI, Air India Ltd. vs. NargeesMeerza, T.M.A. Pai Foundation v. St. of Karnataka, M.C. Mehta vs. UOI etc.,	4 hrs
Chapter No. 2 Relevance of Directive principles of State Policy Relevance of Directive principles of State Policy under Part IV, Fundamental duties & their significance. SarlaMudgal v. UOI	3 hrs
Chapter No. 3 Union Union – President, Vice President, Union Council of Ministers, Prime Minister, Parliament & the Supreme Court of India.	4 hrs
Chapter No.4 State State – Governors, State Council of Ministers, Chief Minister, State Legislature and Judiciary.	2 hrs
Chapter No. 5 Constitutional Provisions for Scheduled Castes & Tribes Constitutional Provisions for Scheduled Castes & Tribes, Women &Children & Backward classes, Emergency Provisions.	2 hrs
Chapter No. 6 Electoral process Electoral process, Amendment procedure, 42nd, 44th and 86th Constitutional amendments.	2 hrs
Unit – 2	
Chapter No. 7 Scope & Aims of Engineering Ethics	5 hrs

Scope & Aims of Engineering Ethics: Meaning and purpose of Engineering Ethics, Responsibility of Engineers, Impediments to responsibility, Honesty, Integrity and reliability, risks, safety & liability in engineering. Bhopal Gas Tragedy, Titanic case.	
Chapter No. 8 Intellectual Property Rights Intellectual Property Rights (IPRs)- Patents, Copyright and Designs	3 hrs
Chapter No. 9 Ethical perspectives of professional bodies Ethical perspectives of professional bodies- IEEE, ASME, NSPE and ABET, ASCE etc.	3 hrs
Unit – 3	
Chapter No. 10 Effects of human activities on environment Effects of human activities on environment - Agriculture, Housing, Industry, Mining, and Transportation activities, Environmental Impact Assessment, Sustainability and Sustainable Development.	2 hrs
Chapter No. 11 Environmental Protection Environmental Protection – Constitutional Provisions and Environmental Laws in India.	2 hrs

Text Books (List of books as mentioned in the approved syllabus)

1. Dr. J. N. Pandey, “Constitutional Law of India”, Central Law Agency, 2005
2. Dr. M.K. Bhandari, “Law relating to Intellectual Property Rights”, Central Law Publications, Allahabad, 2010.
3. Charles E. Harris and others, “Engineering Ethics: Concepts and Cases”, Thomson Wadsworth, 2003

References

1. Durga Das Basu, “Introduction to the Constitution of India”, Prentice-hall EEE, 2001
2. Mike Martin and Ronald Schinzinger, “Ethics in Engineering”, Tata McGraw-Hill Publications.

Back to VII SEM

Course Title: Advanced Digital Logic Design	Course code: 17EECE302	
L-T- P: 0-0-3	Credits: 03	Contact Hrs: 04hrs/week
CIE Marks: 100	SEE Marks: 00	Total Marks: 100
Teaching Hrs: 16hrs Lab Hrs: 24 hrs		

Chapter No. 1. Digital Integrated Circuits Challenges in digital design, Design metrics, Cost of Integrated circuits, ASIC , Evolution of SoC ASIC Flow Vs SoC Flow, SoC Design Challenges. Introduction to CMOS Technology, PMOS & NMOS Operation, CMOS Operation principles, Characteristic curves of CMOS, CMOS Inverter and characteristic curves, Delays in inverters, Buffer Design, Power dissipation in CMOS, CMOS Logic, Stick diagrams and Layout diagrams. Setup time, Hold Time, Timing Concepts.	8 hrs
Chapter No. 2. Digital Building Blocks Decoder, encoder, code converters, Priority encoder, multiplexer, DE multiplexer, Comparators, Parity check schemes, Multiplexer, De-multiplexer, Pass Transistor Logic, application of multiplexer as a multi-purpose logical element. Asynchronous and synchronous up-down counters, Shift registers. FSM Design, Mealy and Moore Modelling, Adder & Multiplier concepts, Memory Concept	6 hrs
Chapter No. 3. Logic Design Using Verilog Evolution & importance of HDL, Introduction to Verilog, Levels of Abstraction, Typical Design Flow, Lexical Conventions, Data Types Modules, Nets, Values, Data Types, Comments, arrays in Verilog, Expressions, Operators, Operands, Arrays, memories, Strings , Delays , parameterized designs Procedural blocks, Blocking and Non-Blocking Assignment, looping, flow Control, Task, Function, Synchronization, Event Simulation. Need for Verification, Basic test bench generation and Simulation	10 hrs
Chapter No. 4. Principles of RTL Design Verilog Coding Concepts, Verilog coding guide lines: Combinational, Sequential, FSM. General Guidelines, Synthesizable Verilog Constructs, Sensitivity List, Verilog Events, RTL Design Challenges, Clock Domain Crossing. Verilog modeling of combinational logic and sequential logic	8 hrs
Chapter No. 5. Design and simulation of Architectural building blocks Basic Building blocks design using Verilog HDL: Arithmetic Components – Adder, Subtractor, and Multiplier design, Data Integrity – Parity Generation circuits, Control logic – Arbitration, FSM Design – overlapping and non-overlapping Mealy and Moore state machine design	8 hrs
Reference Books: 1. Digital Design by Morris Mano M, 4th Edition. 2. Verilog HDL: A Guide to Digital Design and Synthesis by Samir Palnitkar, 2nd Edition. 3. Principles of VLSI RTL Design: A Practical Guide by Sapan Garg, 2011. **Tools:** Questa Sim, NC Verilog, NC Sim, CVER + GTKWave, VCSMX, Modelsim for Verilog	

Back to VI Sem Elective

Course Title: Internet of Things	Course Code: 17EECE307
Total Contact Hours: 3	Duration of ESA: 3 Hours
ISA Marks: 50	ESA Marks: 50

Content	Hrs
Unit - 1	
Chapter No. 1. Introduction to IoT Defining IoT, Characteristics of IoT, What is the IoT and why is it important? Elements of an IoT ecosystem. Technology and business drivers. IoT applications, trends and implications. Physical design of IoT, Logical design of IoT, Functional blocks of IoT, Communication models & APIs	6 hrs
Chapter No. 2. IoT Architecture: State of the Art History of IoT, M2M – Machine to Machine, Web of Things, IoT protocols **Applications:** Remote Monitoring & Sensing, Remote Controlling,Performance Analysis.	4 hrs
Unit - 2	
Chapter No. 3. IoT Communication : The Layering concepts , IoT Communication Pattern, IoT protocol Architecture, The 6LoWPAN,Security aspects in IoT	4 hrs
Chapter No. 4. IoT Application Development: **Application Protocols** MQTT, REST/HTTP, CoAP, MySQL	6 hrs
Unit - 3	
Chapter No. 5. Case Study & advanced IoT Applications: IoT applications in home, infrastructures, buildings, security, Industries, Home appliances, other IoT electronic equipment's. Use of Big Data and Visualization in IoT, Industry 4.0 concepts.	6 hrs

Hands-on Lab

Arduino, Android and AWS based Experiments

1. AWS Setup and instance creation.
2. Controlling LEDs blinking pattern through UART/WiFi
3. Simple photocell to measure the ambient light level
4. Controlling LEDs blinking pattern through PHP web server.
5. Temperature measurement through ADC and WiFi
6. Controlling and interacting with basic actuators (relay).
7. Android Application development.
8. Controlling of Arduino embedded system using Android App.
9. Motor Speed control using Embedded board and NodeMCU

Lua Programming Based Experiments

1. Introduction to Lua programming
2. Controlling inbuilt LED of ESP8266
3. Controlling Motion Sensor using NodeMCU module.
4. Using ESP8266 as Webserver
    a. Understanding HTML Tags.
    b. Understanding Request.
    c. Reading Parameter Values.
    d. Controlling LED.
5. ThingSpeak Cloud - Data Visualization
    a. Working with Temperature & Humidity Sensor
    b. Working with ThingSpeak Cloud
    c. Posting & Analyzing Sensor Data on ThingSpeak Cloud
    d. ThingSpeak Cloud - Mobile App

Working with MQTT/HTTP

1. Introduction to Cloud MQTT
2. MQTT - Wireless Communication between two ESP boards
3. Controlling LED using voice commands - HTTP to MQTT Bridge

Back to VI Sem Elective

Course Title: Information Theory and Coding	Course Code: 21EECE308
Total Contact Hours: 40	Duration of ESA Hours: 3 hours
ESA Marks: 50	ISA Marks: 50

Content	Hrs
Unit - 1	
Chapter 01. Review of information theory: Basics of Information, Measure of information, Entropy.	02 Hrs
Chapter 02. Discrete Channels: Discrete memory less Channels, Mutual information, Channel Capacity, Differential entropy and mutual information for continuous ensembles, Channel capacity Theorem.	08 Hrs
Chapter 03. Source Coding: Encoding of the source output, Shannon's encoding algorithm. Source coding theorem, Binary, ternary and quaternary Huffman coding, Construction of instantaneous codes.	08 Hrs
Unit - 2	
Chapter 04. Introduction to Error Control Coding: Introduction, Types of errors, examples, Types of codes Linear Block Codes: Matrix description, Error detection and correction, Standard arrays and table look up for decoding, Generation of Hamming Codes.	06 Hrs
Chapter 05. Binary Cycle Codes: Algebraic structures of cyclic codes, Encoding using an (n-k) bit shift register, Systematic codes, non systematic codes, Error detection and error correction (Syndrome calculation) circuits.	05 Hrs
Chapter 06. Convolutional codes: Convolution Codes, Time domain approach. Transform domain approach. Systematic Convolution codes, Maximum Likelihood Decoding of Convolutional codes.	05 Hrs
Unit - 3	
Chapter 07. Coding for burst error correction and other types of codes: Burst and random error correcting codes, cyclic codes and convolutional codes for bursts error correction, Reed soloman codes, Cyclic redundancy codes, Golay codes, shortened cyclic codes, Burst error correcting codes. Burst and Random Error correcting codes.	08 Hrs

Text Book (List of books as mentioned in the approved syllabus)

1. K. Sam Shanmugam, Digital and analog communication systems, John Wiley, 1996
2. Simon Haykin, Digital communication, John Wiley, 2003

References

1. Ranjan Bose, ITC and Cryptography, TMH(reprint 2007), 2002
2. Glover and Grant, Digital Communications, 2, Pearson, 2008
3. D Ganesh Rao, K N Haribhat, Digital Communications, Sanguine, 2009

Back to VI Sem Elective

Course Title: Embedded Intelligent Systems			Course Code: 17EECE310
L-T-P: 0-0-3	Credits: 3		Contact Hrs: 6hrs/week
ISA Marks: 80	ESA Marks: 20		Total Marks: 100
Teaching Hrs: 60	Exam Duration: 3 hrs		

	Unit - I	
1	**Basics of embedded systems** Linux Application Programming, System V IPC, . Linux Kernel Internals and Architecture , Kernel Core , Linux Device Driver Programming, Interrupts & Timers , Sample shell script, application program, driver source build and execute	**10 hrs**
2	**Heterogeneous computing** Basics of heterogeneous computing with various hardware architectures designed for specific type of tasks, Advanced heterogeneous computing with a. Introduction to Parallel programming b.GPU programming (OpenCL). Open standards for heterogeneous computing (Openvx) , Basic OpenCL examples - Coding, compilation and execution	**12 hrs**
	Unit - II	
3	**ML Frameworks with the target device** Caffe, tensorflow, TF Lite machine learning frameworks & architecture ,Model parsing, feature support and flexibility ,Supported layers , advantages and disadvantages with each of these frameworks, Android NN architecture overview , Full stack compilation and execution on embedded device	**16 hrs**
4	**Model Development and Optimization** Significance of on device AI, Quantization , pruning, weight sharing, Distillation ,Various pre-trained networks and design considerations to choose a particular pre-trained model ,Federated Learning , Flexible Inferencing	**8 hrs**
	Unit - III	
5	**Android Anatomy** Android Architecture ,Linux Kernel , Binder , HAL Native Libraries , Android Runtime, Dalvik Application framework , Applications, IPC	**8 hrs**

Text Books

1. Linux System Programming , by Robert Love , Copyright © 2007 O'Reilly Media
2. Heterogeneous Computing with OpenCL, 2nd Edition by Dana Schaa, Perhaad Mistry, David R. Kaeli, Lee Howes, Benedict Gaster , Publisher: Morgan Kaufmann

Reference Books:

1. Deep Learning , MIT Press book ,Goodfellow, Bengio, and Courville's
2. Beginning Android , by Wei-Meng Lee , Publisher: Wrox , O'Reilly Media

Scheme for End Semester Assessment (ESA)

UNIT	Experiments to be set of 10 Marks Each	Chapter Numbers	Instructions
I	Project Examination	1,2,3,4,5	Project implementation and demonstration 20 marks

Back to VI Sem Elective

Course Code: 20EECE340	Course Title: Multicore Architecture and Programming	
L-T-P : 2-0-1	Credits: 3	Contact Hrs: 4Hr/week
ISA Marks:50	ESA Marks: 50	Total Marks: 100
Teaching Hrs: 52		Exam Duration: 3

Content	Hrs
Unit – 1	
Chapter No. 1: Introduction to Multicore Drivers for Multicore Architectures: Low power, Performance/Throughput and need for memory bandwidth – Limits of single core computing – Moore's law - Limits to Instruction Level Parallelism (ILP) – Power and heat dissipation issue – Increased amount of data to process – Evolution from traditional System-On-Chip (SoC) to MPSoCs (Multi processor System-On-Chips) - Need for Multicore controllers in Automotive domain	4hrs
Chapter No. 2: Multicore Architecture Dependent Multicore software and hardware architectures –Multicore hardware architecture overview: Heterogeneous and Homogenous Multicore hardware – Communication between hardware processing elements: Point-to-point connections, Shared buses, On-chip cross bar, Network-On-Chip (NoC) - Memory access in Multicore architectures: Symmetric Multi-Processing (SMP), Asymmetric Multi processing aka NUMA (Add pros and cons)– Multicore architecture specific to applications - Example Multicore hardware used in Automotive – Infineon Tricore series, ST devices	12hrs
Unit – 2	
Chapter No. 3: Scheduling concepts and OS aspects What is Scheduling? – Static and Dynamic Scheduling - Scheduling algorithms: Rate Monotonic Scheduling (RMS), Fixed priority preemptive scheduling, Round robin scheduling, Earliest deadline first, first come First serve – Process and threads - What is pre-emption? Why is it needed?- Types of Multicore Scheduling: Global, Semi-partitioned and Partitioned –OS for General purpose and Real time systems - Scheduling in Single core vs Scheduling in Multicore – Timing Jitter	10 hrs
Chapter No. 4: Concurrency and Parallelism Amdahl's law – Need for Parallelism – Concurrency Fundamentals – Data parallelism, Functional Parallelism, loop Parallelism – Dependencies – Producer consumer`— Need for Synchronization, Loop dependencies–Shared resources – Caching aspects - Problems with no synchronization - Synchronization primitives – Semaphore, Mutex, spinlocks, Test and Set, Compare and swap– Synchronization related issues and how to avoid them: Data races, Livelocks, Deadlock, Non-atomic operations –	10hrs

Chapter 5: Advanced Multicore topics – Introduction/Overview Multicore timing analysis - Timing simulation: Why it is needed? – WCET (Worst Case Execution Time) analysis – Schedulability analysis – Additional challenges in Multicore - Tools used in automotive: Timing architect,ChronSIM, Sym TA/S- Deterministic behavior – Logical Execution Time (LET)	4hrs

References:

Highly Recommended: Real world Multicore embedded systems – Bryon Moyer

Highly Recommended for Embedded system and Real Time basics -Programming *Embedded* Systems with C and GNU Development Tools – Michael Barr

References in the internet for Multicore timing analysis:

Why is timing analysis important: http://embedded.cs.uni-saarland.de/publications/EnablingCompositionalityRTNS2016.pdf

Multicore timing simulation solutions:

https://www.vector.com/int/en/events/global-de-en/webinars/2020/timing-analysis-for-multicore-ecus/

https://www.rapitasystems.com/multicore-timing

https://www.inchron.com/tool-suite/chronsim/

https://www.absint.com/ait/symtas.htm

https://www.danlawinc.com/wp-content/uploads/MC-BR-006-Multicore-Timing-Analysis-Solution-For-Aerospace-v3.pdf

Logical Execution Time (LET)

https://ieeexplore.ieee.org/document/5577967

Back to VI Sem Elective

Course Code: 18EECE421	Course Title: OOPS using C++	
L-T-P: 2-0-1	Credits: 3	Contact Hrs: 42
ISA: Marks: 80	ESA Marks: 20	Total Marks: 100
Teaching Hrs: 42		Exam Duration:

Content	Hrs
Unit – 1	
Chapter 1: Fundamental concepts of object oriented programming: Introduction to object oriented programming, Programming Basics (keywords, identifiers, variables, operators, classes, objects),Arrays and Strings, Functions/ methods (parameter passing techniques),	04 hrs
Chapter 2: OOPs Concepts: Overview of OOPs Principles, Introduction to classes & objects ,Creation & destruction of objects, Data Members, Member Functions , Constructor & Destructor , Static class member, Friend class and functions, Namespace	08hrs
Unit – 2	
Chapter 3: Inheritance: Introduction and benefits, Abstract class, Aggregation: classes within classes Access Specifier, Base and Derived class Constructors, Types of Inheritance. Function overriding	8 hrs
Chapter 4: Polymorphism: Virtual functions, Friend functions, static functions, this pointer	6 hrs
Unit – 3	
Chapter 5: Exception Handling: Introduction to Exception, Benefits of Exception handling, Try and catch block, Throw statement, Pre-defined exceptions in C++,Writing custom Exception class	8 hrs
Chapter 6: I/O Streams: C++ Class Hierarchy, File Stream, Text File Handling, Binary File Handling Error handling during file operations, Overloading << and >> operators	6 hrs

Books/References:

Text Book

1. Robert Lafore, "Object oriented programming in C++", 4th Edition, Pearson education, 2009.

References

1. Lippman S B, Lajorie J, Moo B E, C++ Primer, 5ed, Addison Wesley, 2013.
2. Herbert Schildt: The Complete Reference C++, 4th Edition, Tata McGraw Hill

Back to VI Sem Elective

Program: VII Semester Bachelor of Engineering (Electronics & Communication Engineering)		
Course Code: 22EECC401	Course Title: Wireless & Mobile Communication	
L-T-P: 3-0-0	Credits: 3	Contact Hrs: 40
CIE Marks: 50	SEE Marks: 50	Total Marks: 100
Teaching Hrs: 40		Exam Duration: 3 hrs

Content	Hrs
Unit – 1	
Chapter 01: Radio Propagation: Free space propagation model, Relating power to electric field., Relation, ground reflection, scattering, Practical link budget design using path loss model, Outdoor propagation models, Signal penetration into buildings, Ray tracking and site specific modeling, Small scale Multipath measurements, Parameters of mobile Multipath channels, Types of small scale fading.	16
Unit – 2	
Chapter 02: Diversity techniques: Concept of Diversity branch and signal paths, Combining and switching methods, C/N, C/I performance improvements, RAKE receiver.	4
Chapter 03: Cellular concept: Frequency reuse, Channel assignment strategies, Handoff strategies, Interference and system capacity, Trucking and grade of service, Improving coverage, Capacity in cellular systems, FDMA, TDMA, Pseudo noise sequences, notion of spread spectrum, processing gain and Jamming margin, direct sequence spread spectrum, frequency hop spread spectrum ,Spread spectrum multiple access, SDMA packet radio. Capacity of cellular systems.	12
Unit – 3	
Chapter 4: 5G: Implementation, components of the 5G, 5G architecture, 5G design, 5G network, 5G applications, Advantages and disadvantages	4
Chapter 5: Satellite orbits GEO, MEO, LEO and applications. Fiber to the home (FTTH): Working, FTTH architecture and components, benefits, advantages and disadvantages	4

Text Book (List of books as mentioned in the approved syllabus)

1. T.S. Rapport, Wireless Communication, 2, Pearson Education, 2002

References

1. Kamil O Feher, Wireless digital communications: Modulation and spread spectrum Techniques, Prentice Hall of India, 2004

2. Vijay K Garg, IS_95 CDMA and cdma 2000, Pearson publication pvt. Ltd, 2004

3. Xiaodong Wang and Vincent Poor, wireless Communicating system: Advanced Techniques for signal Reception, Pearson publication pvt. Ltd, 2004

Back to VII Electives

Program: VII Semester Bachelor of Engineering (Electronics & Communication Engineering)			Teaching Hours
Course Title: Multimedia Communication		Course Code: 18EECE410	
L-T-P: 2-0-1	Credits: 3	Contact Hours: 3 Hrs/week	
CIE Marks: 50	SEE Marks: 50	Total Marks: 100	
Teaching Hours: 42Hrs	Examination Duration: 3 Hrs		

Unit I	
Chapter 1: Introduction to Multimedia: Multimedia and Hyper media, WWW, overview of multimedia software tools.	02Hrs
Chapter 2: Graphics and Image representation: Graphics / Image data types, Popular file formats.	02Hrs
Chapter 3: Fundamental concepts in video: Types of video signals, analog video, digital video	06Hrs
.**Chapter 4**: Basics of digital audio: Digitization of sound, MIDI, Quantization and transmission of audio.	05Hrs
Unit II	
Chapter 4: Lossless compression algorithms: Introduction, run-length coding, variable length coding, dictionary based coding, arithmetic coding, lossless image compression.	05Hrs
Chapter 5: Lossy compression algorithms: Introduction, distortion measures, quantization, transform coding, wavelet based coding, wavelet packets, embedded zero tree of wavelet coefficients.	06Hrs
Chapter 6: Image compression standards: The JPEG standard, The JPEG2000 standard, The JPEG-LS standard, Bi level image compression standard.	06Hrs
Unit III	
Chapter 7: Basics video compression techniques: Overview, video compression based on motion compensation, H.261	08Hrs
Chapter 8: Overview of MPEG-1, 2 4 and 7.	02Hrs

Text Books

1. Ze-Nian Li & Mark S Drew**, "**Fundamentals of multimedia**"**, Pearson Education, 2004.

References

6. Ralf Steinmetz & Kalra Nahrstedt , "Multimedia: Computing, Communication & Applications", Pearson Education, 2004
7. K R Rao, Zoran S Bojkovic, Dragord A Milovanvic, Pearson education, "Multimedia communication systems: Techniques, Standards, & Networks",. Second Indian reprint, 2004.

Back to VII Electives

Program: VII Semester Bachelor of Engineering (Electronics & Communication Engineering)		
Course Code: 18EECE403	**Course Title: MEMS**	
L-T-P: 3-0-0	**Credits: 3**	**Contact Hrs: 40**
CIE Marks: 50	**SEE Marks: 50**	**Total Marks: 100**
Teaching Hrs: 40		**Exam Duration: 3 hrs**

No	Unit I	Hrs
1	**Overview of MEMS and Microsystems:** Evolution of Microsystems, Miniaturization, Applications of Microsystems in Automotive, Aerospace, Health Care Industry, Industrial Products, Consumer Products and Telecommunications.	05
2	**Working principles of Microsystems:** Micro-sensors: Acoustic wave sensor, Biomedical Sensors and Biosensors, Chemical Sensors Optical Sensors, Pressure Sensors, Thermal Sensors. Micro-actuation: Actuation Using Thermal Forces, Shape Memory Alloys (SMA), Piezoelectric Crystals and Electrostatic Forces. Applications of Micro-actuations: Micro-grippers, Micro-motors, Micro-valves, Micro-pumps.Micro-accelerometers, Micro-fluidics, Numerical Problems.	10
	Unit II	
3	**Scaling laws in miniaturization:** Introduction to scaling, Scaling in Geometry, Rigid-Body Dynamics, Electrostatic Forces, Electromagnetic Forces, Electricity, Fluid Mechanics, Heat Transfer, Numerical problems.	10
4	**Materials for MEMS and Microsystem:** Substrate and Wafers, Active Substrate Materials, Silicon as Substrate Material, Silicon Compounds, Silicon Piezo resistors, Gallium Arsenide, Quartz, Piezoelectric Crystals, Polymers, Packaging Materials.	05

	Unit – III	
5	**Microsystems Fabrication Processes:** Photolithography, Ion Implantation, Diffusion, Oxidation, Chemical Vapor Deposition (CVD), Physical Vapor Deposition (PVD), Etching.	05
6	**Micro-manufacturing:** Bulk Micro-manufacturing, Surface Micromachining, The LIGA Process.	05

Text Book:

*"*MEMS and Microsystems – Design and Manufacture*"*, Tai-Ran Hsu, TMH Edition 2002.

References:

"*Micro system Design*", Stephen D. Senturia, Kluwer Academic Publishers, 2001.

"*Foundations of MEMS*", Chang Liu, Pearson Edition 2012.

"*RF MEMS:Theory, Design, and Technology*", Gabriel M. Rebeiz, John Wiley & Sons Publication, 2003.

Back to VII Electives

Program: VII Semester Bachelor of Engineering (Electronics & Communication Engineering)		
Course Title: **Physical Design-Analog**	***Course code: 18EECE419***	
L-T- P: 0-0-3	***Credits: 03***	***Contact Hrs: 06hrs/week***
CIE Marks: 100	***SEE Marks: 00***	***Total Marks: 100***
Teaching Hrs: 16hrs ***Lab Hrs: 24 hrs***		

Chapter No 1. Standard cell Layout creation: Layout Practice Sessions (DRC/LVS Dirty layout), Understanding verification errors, Error debugging skills, Hands on experience of using layout editor, Quality of the layout, Half DRC rules, Mega module creation.	8 hrs
Chapter No 2. Analog layout: Importance of performance in Analog layout, Importance of floor planning and placement, Attributes need to be taken care during routing stage, Introduction to DRC, LVS, Density and RCX.	8 hrs
Chapter No 3. Matching and Guard rings, Matching: Introduction to mismatch concepts, Causes for mismatch, Types of mismatch, Rules for matching, Activities. Guard ring : What is guard ring, Usage of guard ring	6 hrs
Chapter No 4. Reliability issues: Introduction to failure mechanism, Causes of reliability issues, Process enhancement techniques and Layout considerations to reduce reliability issues	8 hrs
Chapter No 5. Physical design of amplifier and buffer: Applying the studied concepts and doing layout, Prioritising the constraints given, Quality checks, Buddy reviews and implementations, Documentation	10 hrs

Reference:

The Art of Analog Layout – Alan Hastings

CMOS IC layout – Dan Clien

IC Layout Basics – Chris saint and Judy saint

Back to VII Electives

Program: VII Semester Bachelor of Engineering (Electronics & Communication Engineering)			Teaching Hours
Course Title: Digital Image Processing		Course Code: 18EECE414	
L-T-P: 2-0-1	Credits: 3	Contact Hours: 3 Hrs/week	
CIE Marks: 50	SEE Marks: 50	Total Marks: 100	
Teaching Hours: 42Hrs	Examination Duration: 3 Hrs		

Unit I

Chapter 1: Introduction: 2D systems, mathematical preliminaries- FT, Z-transform, Optical and Modulation transfer functions (OTF and MTF). — 04Hrs

Chapter 2: Image perception: Light, luminance, brightness, contrast, MTF of the visual system, visibility function, monochrome vision models, Image fidelity criteria, colour representation, colour models. — 04Hrs

Chapter 3: Image sampling and quantization: 2D sampling theory, limitations in sampling and reconstruction, quantization, optimal quantizer, compandor and visual quantization. — 07Hrs

Unit II

Chapter 4: Image transforms: 2D orthogonal and unitary transforms, DFT, DCT, DST, Hadamard, Harr, Slant, KLT transforms. — 10Hrs

Chapter 5: Image enhancement: Histograms modeling, spatial operations, transform operations, multispectral image enhancement, color image enhancement. — 07Hrs

Unit III

Chapter 6: Image filtering and restoration: Image observation models, Inverse and wiener filtering, fourier domain filters. Smoothing splines and interpolation. SVD and iterative methods. Maximum entropy restoration, Bayesian methods, co-ordinate transformation and geometric corrections. Blind deconvolution. — 10Hrs

Text Books

1. A.K. Jain, ''Fundamentals of Digital Image Processing'', Pearson Education (Asia) Pvt. Ltd

References

1. Rafael C. Gonzalez, Richard E. Woods, “Digital Image Processing”, Pearson Education (Asia) Pvt. Ltd
2. Rafael C. Gonzalez, Richard E. Woods and Steven L Edidins. ''Digital Image Processing Using Matlab'', Pearson Education (Asia) Pvt. Ltd

Back to VII Electives

Program: VII Semester Bachelor of Engineering (Electronics & Communication Engineering)		
Course Code: 18EECE415	**Course Title: Cryptography and Network Security**	
L-T-P: 3-0-0	**Credits: 3**	**Contact Hrs: 42**
CIE Marks: 50	**SEE Marks: 50**	**Total Marks: 100**
Teaching Hrs: 42		**Exam Duration: 3 hrs**

Content	Hrs
Unit - 1	
Chapter No. 1. Overview: Introduction, Services, Mechanisms and attacks of OSI architecture, Model	2 hrs
Chapter No. 2: Introduction to Finite Fields: Groups, Rings and fields. Modular Arithmetic, Euclid's Algorithm, Extended Euclid's algorithm, Finite fields of the form GF (p), Finite fields of the form GF(2n) , Polynomial arithmetic, Euler's and format's theorem, Chinese remainder theorem	4 hrs
Chapter No. 3: Classical Encryption techniques: Symmetric cipher model, substitution technique, Transposition Techniques	5 hrs
Chapter No. 4: Block Ciphers and DES: Design and principles of Block Ciphers,DES, Strength of DES, Block Cipher Modes of Operation	5 hrs
Unit - 2	
Chapter No. 5: Advanced Encryption Standards: Evaluation Criterion of AES, AES Encryption and AES Decryption	4 hrs
Chapter No. 6: Public Key Cryptography and RSA: Design and principles, Concept of confidentiality and Authentication, RSA algorithm, Other Public Key Crypto Systems, Key Management, Daffier Hellman Key Exchange, Elliptic curve Cryptography	6 hrs
Chapter No. 7: Message Authentication and Hash Functions: Message Authentication codes, Hash functions, Security of Hash and MAC functions	3 hrs
Chapter No. 8: Digital Signature, Authentication and Hash Functions: Authentication Protocols, Digital signature Standard, DSS Algorithm	3 hrs

Unit - 3	
Chapter No. 9. Electronic Mail Security: Pretty good privacy, Data Compression, PGP random number generator	3 hrs
Chapter No. 10. IP Security & Web Security IP security Architecture, Security Associations, Key management , Web security Considerations, Secure Socket layer, Transport layer security, secure electronic transactions	7 hrs

Text Book (List of books as mentioned in the approved syllabus)

1. William Stallings, Cryptography and Network Security-Principles and practices, 3rd, PHI, 2003
2. Atul Kahate , Cryptography and Network Security , TMH, 2003
3. Behrouz A. Forouzan, Cryptography and Network Security, TMH, 2007

References

1. Koeblitz, Introduction to Number theory and Cryptography , Springler, 0000
2. Bruce Schneider, Applied Cryptography, 2nd , John Wiley, 2001
3. Eric Maiwad, Fundamentals of Network security, 2nd , TMH, 2002

Back to VII Electives

Program: VII Semester Bachelor of Engineering (Electronics & Communication Engineering)			Teaching Hours
Course Title: Embedded Linux		Course Code: 18EECE405	
L-T-P: 3-0-0	Credits: 3	Contact Hours: 3 Hrs/week	
CIE Marks: 50	SEE Marks: 50	Total Marks: 100	
Teaching Hours: 42Hrs	Examination Duration: 3 Hrs		

Unit I

Chapter 1: Introduction to Embedded Linux: — 04 Hrs

A Brief History of Linux -Benefits of Linux -Acquiring and Using Linux -Examining Linux Distributions - Devices and Drives in Linux-Components: Kernel, Distribution, Sawfish, and Gnome. — 06 Hrs

Chapter 2: Overview of Embedded Linux: — 06 Hrs

Overview: Development-Kernel architectures and device driver model- Embedded development issues-Tool chains in Embedded Linux-GNU Tool Chain (GCC,GDB, MAKE, GPROF & GCONV)- Linux Boot process.

Chapter 3: System Management and user interface

Boot sequence-System loading, sys linux, Lilo, grub-Root file system-Binaries required for system operation-Shared and static Libraries overview-Writing applications in user space-GUI environments for embedded Linux system

Unit II

Chapter 4: File system in Linux: — 06 Hrs

File system Hierarchy-File system Navigation -Managing the File system –Extended file systems-INODE-Group Descriptor-Directories-Virtual File systems- Performing File system Maintenance -Locating Files –Registering the File systems- Mounting and Un-mounting –Buffer cache-/proc file systems-Device special files — 04 Hrs

Chapter 5:Configuration:

Configuration, Compilation & Porting of Embedded Linux-Examining Shells -Using Variables - Examining Linux Configuration Script Files -Examining System Start-up Files -Creating a Shell Script — 08 Hrs

Chapter 6: Process management and Inter process communication:

Managing Process and Background Processes -Using the Process Table to Manage Processes - Introducing Delayed and Detached Jobs - Configuring and Managing Services -Starting and Stopping Services -Identifying Core and Non-critical Services -Configuring Basic Client Services - Configuring Basic Internet Services –Working with Modules.

IPC-Benefits of IPC- Basic concepts-system calls-creating pipes-creating a FIFO-FIFO operations-IPC identifiers-IPC keys-IPCS commands- Message queues-Message buffer-Kernel Ring Buffer semaphores-semtools-shared memory semtools- signals-sockets

Unit III	
Chapter 7: Linux device drivers Devices in Linux- User Space Driver APIs- Compiling, Loading and Exporting- Character Devices- Tracing and Debugging- Blocking and Wait Queues- Accessing Hardware- Handling Interrupts- Accessing PCI hardware- USB Drivers- Managing Time- Block Device Drivers- Network Drivers- Adding a Driver to the Kernel Tree.	08 Hrs

Text Books

1.Embedded Linux –Hardware, Software and Interfacing - Craig Hollabaugh, Addison-Wesley Professional, 2002

2.Embedded / Real-Time Systems: Concepts, Design and Programming Black Book, New ed (MISL-DT) Paperback – 12 Nov 2003.

References

3.Building Embedded Linux Systems, Karim Yaghmour, First edition, April 2003.

4. Embedded Linux- John Lombardo, Newriders.com

Back to VII Electives

Program: VII Semester Bachelor of Engineering (Electronics & Communication Engineering)		
Course Code: 18EECE409	Course Title: Design and Analysis of Algorithms	
L-T-P: 0-0-3	Credits: 3	Contact Hrs: 72 Hrs
ISA Marks: 100	ESA Marks: 00	Total Marks: 100

Content	
Unit – 1	**Hrs**
Chapter No. 1 : Framework for Analysis of Algorithm Efficiency Analysis Framework, Asymptotic Notations and Basic Efficiency Classes, Mathematical Analysis of Non-Recursive Algorithms, Mathematical Analysis of Recursive Algorithms.	**4**
Chapter No 2: Trees and Graphs Overview of Trees. AVL Trees. Red – Black Trees. Graphs, DFS and its applications, BFS and its applications. Topological Sorting. Shortest path algorithms. Minimum Spanning Tree.	**8**
Chapter No 3 : Hashing Direct Address Table, Hash Table, Hash Function, Collision Resolution Techniques.	**3**
Unit – 2	
Chapter No 4 : Substring Matching and Sorting Techniques. Brute-force method, Boyer-Moore – Hoorspool Algorithm, Knuth-Morris-Pratt Algorithm, Bubble sort, selection sort. Divide and Conquer: insertion sort, merge sort, quick sort and heap sort	**8**
Chapter No 5: Greedy Technique Introduction, Interval Scheduling, Proof Strategies, Huffmann Coding, 0/1 knapsack	**2**
Chapter No 6: Dynamic Programming Introduction and Definition. Memorization, Fibonacci Series, Edit Distance, Longest Increasing Subsequence, Longest Common Subsequence, Matrix multiplication, Coin Change problem, Subset Sum problem.	**5**
Unit - 3	
Chapter No 7 : Backtracking Introduction. N-Queens Problem, Generating string permutation, Hamiltonian Cycle.	**5**
Chapter No 8 : Branch and Bound Introduction. Travelling Salesman problem, Job Assignment Problem.	**5**

Text Books:

1. Data Structures with C -- Seymour Lipschutz, Schaum's Outline Series
2. Introduction to Design and Analysis of Algorithms – Anany Levitin 3rd Edition

Reference Books:

1. Introduction to Algorithms – Thomas H. Cormen 3rd edition
2. Data Structures, Algorithms and Applications In C++ -- Satraj Sahani
3. Data Structures and Algorithms Made Easy – Narshiman Karumunchi, Career Monk

Back to VII Electives

Program: VII Semester Bachelor of Engineering (Electronics & Communication Engineering)		
Course Title: Advanced Digital Logic Verification	**Course code: 18EECE418**	
L-T- P: 0-0-3	**Credits: 03**	**Contact Hrs: 06hrs/week**
CIE Marks: 100	**SEE Marks: 00**	**Total Marks: 100**
Teaching Hrs: 16hrs **Lab Hrs: 24 hrs**		

Chapter No. 1. Verification Concepts: Concepts of verification, importance of verification, Stimulus vs Verification, functional verification, test bench generation, functional verification approaches, typical verification flow, stimulus generation, direct testing, Coverage: Code and Functional coverage, coverage plan.	8 hrs
Chapter No. 2. Language Constructs System Verilog constructs: Data types: two-state data, strings, arrays: queues, dynamic and associative arrays, Structs, enumerated types. Program blocks, module, interfaces, clocking blocks, modports.	6 hrs
Chapter No. 3. Classes & Randomization SV Classes: Language evolution, Classes and objects, Class Variables and Methods, Class instantiation, Inheritance, and encapsulation, Polymorphism. Randomization: Directed Vs Random Testing. Randomization: Constraint Driven Randomization.	10 hrs
Chapter No. 4. Assertions & Coverage Assertions: Introduction to Assertion based verification, Immediate and concurrent assertions. Coverage driven verification: Motivation, Types of coverage, Cover Group, Cover Point, Cross Coverage, Concepts of Binning and event sampling.	8 hrs
Chapter No. 5. Building Testbench: Layered testbench architecture. Introduction to Universal Verification Methodology, Overview of UVM Base Classes and simulation phases in UVM and UVM macros. Unified messaging in UVM, UVM environment structure, Connecting DUT- Virtual Interface	8 hrs

References:

1. System Verilog LRM
2. Chris Spear, Gregory J Tumbush - SystemVerilog for verification - a guide to learning the testbench language features - Springer, 2012
3. Step-by-Step Functional Verification with SystemVerilog and OVM by Sasan Iman SiMantis Inc. Santa Clara, CA Spring 2008

Tools: Questa Sim, NC Verilog, NC Sim, CVER + GTKWave, VCSMX, Modelsim for Verilog

Back to VII Electives

Program: VII Semester Bachelor of Engineering (Electronics & Communication Engineering)		
Course Title: CMOS ASIC Design (PD-Digital)	**Course code: 18EECE420**	
L-T- P: 0-0-3	**Credits: 03**	**Contact Hrs: 06hrs/week**
CIE Marks: 100	**SEE Marks: 00**	**Total Marks: 100**
Teaching Hrs: 40hrs **Lab Hrs: 24 hrs**		

Chapter No. 1. Introduction: Design of combinational and sequential logic gates in CMOS. Layout and characterization of standard cells. Verilog for representing gate level netlists.	8 hrs
Chapter No. 2. Timing Analysis: Sequential circuit timing and static timing analysis. Cell and net delays and cross-talk. Rationale and implementation of scan chains for testing standard-cell based logic circuits. Timing Verification: Setup Timing Check, Hold Timing Check, Timing across Clock Domains	10hrs
Chapter No. 3: Physical design Physical design of standard-cell based CMOS ASICs: scan insertion, placement, and clock tree synthesis and routing. Netlist transformations at each step of the physical design process. Net parasitic and parasitic extraction. Use of PLLs for clock generation and de-skew.	12 hrs
Chapter No. 4. Standard Data formats: Standard data formats for representing technology and design: LEF, Liberty, SDC, DEF and SPEF. Clock gating and power gating for reduction of device power consumption. Design for reliability: electro- migration, wire self heat and ESD checks and fixes.	6 hrs
Chapter No. 5. Packaging An overview of package design and implementation and system level timing.	4 hrs

Reference Books:

1. The Design & Analysis of VLSI Circuits, L. A. Glassey & D. W. Dobbepahl, Addison Wesley Pub Co. 1985.
2. H. Bhatnagar, Advanced ASIC Chip Synthesis Using Synopsys Design Compiler Physical Compiler and PrimeTime, 2nd edition, 2001.
3. Static Timing Analysis for Nanometer Designs A Practical Approach, J. Bhasker • Rakesh Chadha, Springer Science+Business Media, LLC 2009

Tools: Cadence Innovous, Encounter

Back to VII Electives

Program: VII Semester Bachelor of Engineering (Electronics & Communication Engineering)		
Course Code: 18EECE411	**Course Title: Microwave & Antenna**	
L-T-P: 3-0-0	**Credits: 03**	**Contact Hrs: 40**
CIE Marks: 50	**SEE Marks: 50**	**Total Marks: 100**
Teaching Hrs: 40		**Exam Duration: 03 hrs**

Content	Hrs
Unit - 1	
Chapter No. 1. Microwave Vacuum Tube Devices: Introduction , Reflex Klystron , Problems	**04**
Chapter No. 2. Microwave components: Directional couplers, Circulators, Magic T, Isolator, s-Matrix and Attenuators	**08**
Unit - 2	
Chapter No. 3. Antenna Parameters: Introduction**,** Basic antenna parameters ,Pattern, Beam width, Radiation intensity, Beam efficiency, Directivity, Gain, Aperture, Effective height, Polarization, Antenna field zone, The radio communication link. Radiation resistance of Short electric dipole and half wave length antenna.	**10**
Chapter No. 4. Sources and Arrays: Introduction, Point sources, Power patterns, Power theorem, Examples on power theorem, Directivity and beam width of point sources, Arrays of two isotropic point sources, Pattern multiplication, Linear array of n isotropic point sources of equal amplitude and spacing, Broad side array, End fire array.	**08**
Unit - 3	
Chapter No. 5. Antenna practice: Yagi-Uda Antenna, Loop antenna, Horn antenna, Parabolic reflector, Helical antenna, Log periodic antenna, Mobile Station Antennas, Antennas for GPR : Pulse Bandwidth, Embedded Antennas, UWB Antennas for Digital Applications, The Plasma Antenna	**10**

Text Book (List of books as mentioned in the approved syllabus)

1. J.D.Kraus & Khan,MGH publication ,“Antennas” , 2006, third edition.
2. Samuel Y Liao, “Microwave Devices and Circuits”, PHI Pearson Education, Third Edition.

References

1. F.E.Terman, “Electromagnetic and radio engineering” by, TMcH publication, second Edition.
2. E.C.Jordan’, “Electromagnetic waves & radiating systems” , PHI publication, second edition
3. C.A.Balnis, “Antenna theory and analysis and design” ,1999,third edition.
4. K.D.Prasad ,“Antenna and wave propagation” by ‘1990, first edition.
5. Annapurna Das, Sisir K Das ,“Microwave engineering” , TMH Publications 2001.

Back to VII Electives

Program: VII Semester Bachelor of Engineering (Electronics & Communication Engineering)		
Course Code: 19EECE416	Course Title: Biosensor	
L-T-P: 0-0-3	Credits: 3	Contact Hrs: 72
ISA Marks: 100	ESA Marks: 00	Total Marks: 100
Teaching Hrs: 72		Exam Duration: 3 hrs

Content	Hrs
Unit - 1	
Chapter No. 1. Basic Introduction to sensors: Introduction to sensors: fundamental characteristics such as Sensitivity, linearity, repeatability, hysteresis, drift. Sensing Principles: optical sensors, electrochemical sensors, micromechanical sensors, surface Plasmon sensors, colorimetric Sensors, acoustic sensors	5 hrs
Chapter No. 2. Active Electrical Transducers: Thermoelectric transducers, thermoelectric phenomenon, common thermocouple systems, piezoelectric transducers, piezoelectric phenomenon piezoelectric materials, piezoelectric force transducers, piezoelectric strain, piezoelectric torque transducers, piezoelectric pressure transducers, piezoelectric acceleration transducers. Magnetostrictive transducers Magnetostrictive force transducers, Magnetostrictive acceleration transducers, Magnetostrictive torsion transducers, Hall Effect transducers, and application of Hall transducer. Electromechanical Transducers-Tachometers, variable reluctance tachometers Electrodynamic vibration transducers, Electromagnetic pressure electromagnetic flowmeter. Photoelectric transducers- photoelectric phenomenon, photoelectric transducers, Photo volatile transducers, Photo emissive transducers. Electrochemical transducers- basics of electrode potentials, reference electrodes, indicator electrodes, measurement of PH, measurement of bioelectric signals.	10 hrs
Unit - 2	
Chapter No. 3. Passive electrical transducer: Introduction, Resistive transducers- resistance thermometers, hot wire resistance transducers, Resistive displacement transducer, Resistive strain transducer, resistive pressure transducer, resistive optical radiation transducers. Inductive Transducers-Inductive thickness transducers, Inductive displacement transducers, Movable core-type Inductive transducers, eddy current type Inductive transducers. Capacitive transducers-Capacitive thickness transducers, capacitive displacement transducers, capacitive moisture transducers Substrate and Wafers, Active Substrate Materials, Silicon as Substrate Material, Silicon Compounds, Silicon Piezo resistors, Gallium Arsenide, Quartz, Piezoelectric Crystals, Polymers, Packaging Materials.	5 hrs
Chapter No. 4. Micro fabrication Technology: Design of process flow for device fabrication for application in biology and medicine: Introduction to the Clean room and contaminants, Wafer cleaning processes (DI water, RCA, metallic impurities, etc.), Substrate materials: Silicon, polymer and PCB, Thermal oxidation: Wet and dry oxidation, thin film deposition techniques: PVD- DC and RF Magnetron Sputtering, thermal evaporation, e-beam evaporation, LPCVD, PLD. Types of masks: Hard and soft Lithography, Lithography – UV Photolithography, Soft lithography,	10 hrs

additive manufacturing. Mask design and fabrication – Photo resists and mechanical mask such as stencils. Types of etching- Wet etching- anisotropic and Isotropic and dry etching RIE and DRIE. Device fabrication and inspection in the clean room.	
Unit - 3	
Chapter No. 5. Biosensors Introduction: Biosensors and its applications in health care, agriculture, drug discovery and environmental monitoring. Devices for biology and medicine: Microfluidic channels, flow cytometry/ sorting, microchip using electrophoresis, force measurement with cantilevers, micro engineered devices for medical therapeutics, blood pressure sensors, devices for drug delivery, and devices for minimally invasive surgery.	5 hrs
Chapter No. 6. Biological components for detection Enzymes, antigen-antibody reaction, biochemical detection of analysts, organelles, whole cell, receptors, DNA probe, pesticide detection, sensors for pollutant gases. Surface chemistry: Immobilization of biorecognition element, Antigen-Antibody functionalization, and assay labels including radioisotopes, fluorophores, dyes.	5 hrs

Text Books (List of books as mentioned in the approved syllabus):

1. Fundamentals of Microfabrication and Nanotechnology by Marc J. Madou, 3rd edition. Taylor and Francis group.
2. Transducers and Instrumentation – D.V.S. Murthy, 2nd Edn, PHI Ltd, 2010.
3. A.P.F. Turner, I. Karube & G.S. Wilson: Biosensors: Fundamentals & Applications, Oxford University Press, Oxford, 1987.

References:

1. Ernest O. Doeblin : Measurement Systems, Application and Design, McGraw-Hill, 1985.
2. Richard S.C. Cobbold : Transducers for Biomedical Measurements: Principles and Applications, John Wiley & Sons, 1974
3. John G. Webster (ed.) : Medical Instrumentation - Application and Design; Houghton Mifflin Co., Boston, 1992.
4. Stephen D. Senturia : "Micro system Design", Kluwer Academic Publishers, 2001

Back to VII Electives

Program: VII Semester Bachelor of Engineering (Electronics & Communication Engineering)		
Course Code: 20EECE406	Course Title: AUTOSAR	
L-T-P : 3-0-0	Credits: 3	Contact Hrs: 3 Hours
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hrs: 40		Exam Duration: 3

Content	Hrs
Unit - 1	
Chapter No. 1: AUTOSAR Fundamentals: Evolution of AUTOSAR – Motivations and Objectives AUTOSAR consortium – Stake holders – work Packages, AUTOSAR Partnership, Goals of the partnership, Organization of the partnership, AUTOSAR specification, AUTOSAR Current development status, BSW Conformance classes: ICC1, ICC2, ICC3, and Drawbacks of AUTOSAR.	8 hrs
Chapter No. 2: AUTOSAR layered Architecture: AUTOSAR Basic software, Details on the various layers , Details on the stacks Virtual Function Bus (VFB) Concept Overview of AUTOSAR Methodology , Tools and Technologies for AUTOSAR AUTOSAR Application Software Component (SW-C) ,Types of SW-components AUTOSAR Run Time Environment (RTE): RTE Generation Process: Contract Phase, Generation Phase, MCAL, IO HW Abstraction Layer, Partial Networking, Multicore, J1939 Overview, AUTOSAR Ethernet, AUTOSAR E2E Overview , AUTOSAR XCP, Metamodel , From the model to the process , Software development process.	7 hrs
Unit - 2	
Chapter No. 3: Methodology of AUTOSAR and Communication in AUTOSAR: CAN Communication, CAN FD, CANape, Application Layer and RTE, intra and inter ECU communication, Client-Server Communication, Sender-Receiver, Communication, CAN Driver, Communication Manager (ComM), Overview of Diagnostics Event and Communication Manager	10 hrs
Chapter No. 4: Overview about BSW constituents: BSW Constituents: Memory layer, COM and Services layer, ECU abstraction, AUTOSAR, Operating system, Interfaces: Standard interface, AUTOSAR standardized interface, BSW-RTE interface,(AUTOSAR interface), BSW-ECU hardware interface, Complex device drivers and BSW module configuration, AUTOSAR Integration.	5 hrs
Unit - 3	
Chapter 5: MCAL and ECU abstraction Layer: Microcontroller Drivers, Memory drivers: on-chip and off chip drivers, IO drivers(ADC, PWM, DIO), Communication drivers: CAN driver, LIN drivers, Flexrfay	5 hrs
Chapter 6: Service Layer: Diagnostic Event Manager, Function inhibits Manager, Diagnostic communication manager, Network management, Protocol data unit router, Diagnostic log and trace unit, COMM manager.	5 hrs
Text Book (List of books as mentioned in the approved syllabus) 1. Ronald K. Jurgen, Infotainment systems, 2007, SAE International, 2007	

Back to VII Electives

Program: VII Semester Bachelor of Engineering (Electronics & Communication Engineering)		
Course Code: 21EECE421	**Course Title: RF VLSI**	
L-T-P : 3-0-0	**Credits: 3**	**Contact Hrs: 3 Hours**
ISA Marks: 50	**ESA Marks: 50**	**Total Marks: 100**
Teaching Hrs: 40		**Exam Duration: 3**

Content	Hrs
Unit - 1	
Chapter No. 1: Basic concepts in RF Design Basic concepts in RF Design – harmonics, gain compression, desensitization, blocking, cross modulation, intermodulation, inter symbol interference, noise figure, Friis formula, sensitivity and dynamic range.	8 hrs
Chapter No. 2: Receiver architectures Receiver architectures – heterodyne receivers, homodyne receivers, image-reject receivers, digital-IF receivers and subsampling receivers.	7 hrs
Unit - 2	
Chapter No. 3: Transmitter architectures Transmitter architectures – direct-conversion transmitters, two-step transmitters; Low noise amplifier (LNA) – general considerations, input matching, CMOS LNAs	10 hrs
Chapter No. 4: Mixers Down conversion mixers – general considerations, spur-chart, CMOS mixers	5 hrs
Unit - 3	
Chapter 5: Oscillators Oscillators – Basic topologies, VCO, phase noise, CMOS LC oscillators; PLLs – Basic concepts, phase noise in PLLs, different architectures	10 hrs

Text Books:

Behzad Razavi, RF Microelectronics, Prentice Hall PTR, 1997

Thomas H. Lee, The design of CMOS radio-frequency integrated circuit, Cambridge University Press, 2006

Chris Bowick, RF Circuit Design, Newnes, 2007

Back to VII Electives

Program: VII Semester Bachelor of Engineering (Electronics & Communication Engineering)		
Course Code: 21EECE423	**Course Title: CAD for VLSI**	
L-T-P : 3-0-0	**Credits: 3**	**Contact Hrs: 3 Hours**
ISA Marks: 50	**ESA Marks: 50**	**Total Marks: 100**
Teaching Hrs: 40		**Exam Duration: 3**

Content	Hrs
Unit - 1	
Chapter No. 1: Introduction Introduction to VLSI design methodologies and supporting CAD environment. Schematic editors: Parsing: Reading files, describing data formats, Graphics & Plotting Layout. Layout Editor: Turning plotter into an editor. Layout language: Parameterized cells, PLA generators.	8 hrs
Chapter No. 2: Silicon Compiler Introduction to Silicon compiler, Data path, Compiler, Placement & routing, Floor planning.	7 hrs
Unit - 2	
Chapter No. 3: Layout Analysis and Simulations Layout Analysis: Design rules, Object based DRC, Edge based layout operations. Module generators. Simulation: Types of simulation, Behavioral simulator, logic simulator, functional simulator & Circuit simulator. Simulation Algorithms: Compiled code and Event-driven. Optimization Algorithms: Greedy methods, simulated annealing, genetic algorithm and neural models.	10 hrs
Chapter No. 4: Testing ICs Testing ICs: Fault simulation, Aids for test generation and testing. Computational complexity issues: Big Oh and big omega terms.	5 hrs
Unit - 3	
Chapter 5: Recent Topics in CAD-VLSI Recent topics in CAD-VLSI: Array compilers, hardware software co-design, high-level synthesis tools and VHDL modeling.	10 hrs

Text Books:

1. Stephen Trimberger," Introduction to CAD for VLSI", Kluwer Academic publisher, 2002

2. Naveed Shervani, "Algorithms for VLSI physical design Automation", Kluwer Academic Publisher, Second edition.

Reference Books

1. Gaynor E. Taylor, G. Russell, "Algorithmic and Knowledge Based CAD for VLSI", Peter peregrinus ltd. London.
2. Gerez, "Algorithms VLSI Design Automation", John Wiley & Sons.

Back to VII Electives

Program: VII Semester Bachelor of Engineering (Electronics & Communication Engineering)		
Course Code: 21EECE424	Course Title: System on Chip Design	
L-T-P : 3-0-0	Credits: 3	Contact Hrs: 3 Hours
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hrs: 40		Exam Duration: 3

Content	Hrs
Unit - 1	
Chapter No. 1: Introduction Introduction: Driving Forces for SoC - Components of SoC - Design flow of SoC Hardware/Software nature of SoC - Design Trade-offs - SoC Applications	5 hrs
Chapter No. 2: System Level Design System-level Design: Processor selection-Concepts in Processor Architecture: Instruction set architecture (ISA), elements in Instruction Handing-Robust processors: Vector processor, VLIW, Superscalar, CISC, RISC—Processor evolution: Soft and Firm processors, Custom Designed processors- on-chip memory.	10 hrs
Unit - 2	
Chapter 3: On-chip bus and IP based design Interconnection: On-chip Buses: basic architecture, topologies, arbitration and protocols, Bus standards: AMBA, Core Connect, Wishbone, Avalon - Network-on chip: Architecture topologies-switching strategies - routing algorithms flow control, Quality-of-Service- Reconfigurability in communication architectures. IP based system design: Introduction to IP Based design, Types of IP, IP across design hierarchy, IP life cycle, Creating and using IP - Technical concerns on IP reuse – IP integration - IP evaluation on FPGA prototypes.	10 hrs
Chapter 4: SoC Implementation SOC implementation: Study of processor IP, Memory IP, wrapper Design - Real-time operating system (RTOS), Peripheral interface and components, High-density FPGAs - EDA tools used for SOC design.	5 hrs
Unit - 3	
Chapter 5: SoC Testing SOC testing: Manufacturing test of SoC: Core layer, system layer, application layer-P1500 Wrapper Standardization-SoC Test Automation (STAT).	10 hrs

Text Books:

1. Michael J.Flynn, Wayne Luk, “Computer system Design: Systemon-Chip”, Wiley-India, 2012.
2. Sudeep Pasricha, Nikil Dutt, “On Chip Communication Architectures: System on Chip Interconnect”, Morgan Kaufmann Publishers, 2008.
3. W.H.Wolf, “Computers as Components: Principles of Embedded Computing System Design”, Elsevier, 2008.

Reference Books

1. Patrick Schaumont “A Practical Introduction to Hardware/Software Co-design”, 2nd Edition, Springer, 2012.
2. Lin, Y-L.S. (ed.), “Essential issues in SOC design: designing complex systems-on-chip. Springer, 2006.
3. Wayne Wolf, “Modern VLSI Design: IP Based Design”, Prentice-Hall India, Fourth edition, 2009.

Back to VII Electives

Program: VII Semester Bachelor of Engineering (Electronics & Communication Engineering)		
Course Code: 21EECE422	**Course Title: Speech Processing**	
L-T-P : 3-0-0	**Credits: 3**	**Contact Hrs: 3 Hours**
ISA Marks: 50	**ESA Marks: 50**	**Total Marks: 100**
Teaching Hrs: 40		**Exam Duration: 3**

Content	Hrs
Unit - 1	
Chapter 1: Introduction: Basic Concepts: Speech Fundamentals: Articulatory Phonetics – Production and Classification of Speech Sounds; Acoustic Phonetics – acoustics of speech production; Review of Digital Signal Processing concepts; Short-Time Fourier Transform, Filter-Bank and LPC Methods.	5 hrs
Chapter 2: Speech Analysis: Features, Feature Extraction and Pattern Comparison Techniques: Speech distortion measures – mathematical and perceptual – Log Spectral Distance, Kestrel Distances, Weighted Kestrel Distances and Filtering, Likelihood Distortions, Spectral Distortion using a Warped Frequency Scale, LPC, PLP and MFCC Coefficients, Time Alignment and Normalization – Dynamic Time Warping, Multiple Time – Alignment Paths.	10 hrs
Unit - 2	
Chapter 3: Speech Modeling: Hidden Markov Models: Markov Processes, HMMs – Evaluation, Optimal State Sequence – Viterbi Search, Baum-Welch Parameter Re-estimation, Implementation issues	10 hrs
Chapter 4: Speech Recognition: Large Vocabulary Continuous Speech Recognition: Architecture of a large vocabulary continuous speech recognition system – acoustics and language models – n-grams, context dependent sub-word units; Applications and present status.	5 hrs
Unit - 3	
Chapter 5: Speech Synthesis Text-to-Speech Synthesis: Concatenative and waveform synthesis methods, subword units for TTS, intelligibility and naturalness – role of prosody, Applications and present status.	10 hrs

Text Books:

1. Lawrence Rabinerand Biing-Hwang Juang, “Fundamentals of Speech Recognition”, Pearson Education, 2003.
2.Daniel Jurafsky and James H Martin, “Speech and Language Processing – An Introduction to Natural Language Processing, Computational Linguistics, and Speech Recognition”, Pearson Education.

Reference Books

1.Steven W. Smith, “The Scientist and Engineer’s Guide to Digital Signal Processing”, California Technical Publishing.
2.Thomas F Quatieri, “Discrete-Time Speech Signal Processing – Principles and Practice”, Pearson Education.
3.Claudio Becchetti and Lucio Prina Ricotti, “Speech Recognition”, John Wiley and Sons, 1999.
4.Ben gold and Nelson Morgan, “Speech and audio signal processing”, processing and perception of speech and music, Wiley- India Edition, 2006 Edition.
5.Frederick Jelinek, “Statistical Methods of Speech Recognition”, MIT Press.

Back to VII Electives

Program: VII Semester Bachelor of Engineering (Electronics & Communication Engineering)		
Course Code: 22EECE423	**Course Title: Power Management Integrated Circuit**	
L-T-P: 3-0-0	**Credits: 3**	**Contact Hrs: 40**
ISA Marks: 50	**ESA Marks: 50**	**Total Marks: 100**
Teaching Hrs: 40		**Exam Duration: 3 hrs**

Content	Hrs
Unit – 1	
Chapter 1. Basic Concepts of Power Management Introduction to Power Management; Performance Parameters. Sub-1-volt Bandgap Reference;	6 hrs
Chapter 2. Linear Regulators Introduction to Linear Regulator, Applications of Linear Regulator; : Miller Compensation, R.H.P. zero due to Miller Compensation, Intuitive Methods of Determining Poles and Zeros after Miller Compensation, Static Offset Correction, Dynamic Offset Cancellation; Digital LDO, Avoidance of Limit Cycle Oscillations in a Digital LDO, : Hard Switching Loss, Magnetic Loss, Relative Significance of Losses as a Function of the Load Current	12 hrs
Unit – 2	
Chapter 4. Buck Converters Compensating a Voltage-Mode-Controlled Buck Converter; Designing Type-I (Integral), Type-II (PI) and Type-III (PID) Compensators; Designing Type-III Compensator using Gm-C Architecture and Design Example, Designing the Gate-Driver (Gate Buffer and Non-Overlap Clock Generator) Non-Linear Control Techniques for DC-DC Converters; Hysteretic Control	12hrs
Unit – 3	
Chapter 7. PMIC Layout Selecting the Process Node for a PMIC, Board-Level Layout Guidelines, EMI Considerations Introduction to Advanced Topics in Power Management	10hrs

Text Books (List of books as mentioned in the approved syllabus):

1. Switch-Mode Power Supplies: SPICE Simulations and Practical Designs by Christophe P. Basso, McGraw-Hill Professional, 2008.

2. Fundamentals of Power Electronics, 2nd edition by Robert W. Erickson, Dragan Maksimovic, Springer, 2001.

3. Power Management Techniques for Integrated Circuit Design By Ke-Horng Chen, Wiley-Blackwell, 2016.

4. Design of Analog CMOS Integrated Circuits by Behzad Razavi, McGraw-Hill, 2017.

Back to VII Electives

Program: VII Semester Bachelor of Engineering (Electronics & Communication Engineering)		
Course Code: 22EECE424	**Course Title: Virtualization and Cloud Computing**	
L-T-P: 3-0-0	**Credits: 03**	**Contact Hrs: 03**
ISA Marks: 50	**ESA Marks: 50**	**Total Marks: 100**
Teaching Hrs: 42		**Exam Duration: 03hrs**

Content	Hours
Unit – 1	
Chapter 1. Cloud Computing: Concept, Definition, Cloud Types and Service Deployment Models	05hrs
Chapter 2. Virtualization: Concept, Definition, Types of Virtualization, Hardware Virtualization, Full and Para Virtualization, Hypervisors, Hardware-assisted virtualization, operating system level virtualization, application virtualization	10hrs
Unit – 2	
Chapter 3. Virtual and Physical Networking: Introduction, Switches, virtual NICs, Virtual Networking, virtual LAN	05hrs
Chapter 4. Storage Virtualization: Introduction, SAN/NAS versus storage virtualization.	04hrs
Chapter 5 Virtual Machine Management: Base Virtual Machine, Virtual CPUs, Sockets, Cores, Memory Scaling Up and Scaling Down, USB Support, Virtual Disks, Live Migration. Security	06hrs
Unit – 3	
Chapter 6. Containers: Concept, Definition, Ducker, Container versus Virtualization, Portability, Remote deployment	06hrs
Chapter 7 Applications and Case Studies: Linux KVM, Virtual Box, Open stack	06hrs

Text Book (List of books as mentioned in the approved syllabus)

1. D.E. SARNA (2010), Implementing and Developing Cloud Computing Applications, CRC Press.
2. B.S. SODHI (2017), Topics in Virtualization and Cloud Computing, Ropar PB India, 2017.

References

1. B. FURHT, A. ESCALANTE (2010), Handbook of Cloud Computing (Vol. 3), Springer.

Back to VII Electives

Program: VII Semester Bachelor of Engineering (Electronics & Communication Engineering)		
Course Code: 21EECE425	Course Title: Computer Graphics(IITD-Online)	
L-T-P: 0-0-3	Credits: 03	Contact Hrs: 03
ISA Marks: 100	ESA Marks: -	Total Marks: 100
Teaching Hrs: 42		Exam Duration: 03hrs

Content	Hours
Prof. Saurabh Saxena, IIT Madras NPTEL 12 Weeks (Starts: 25-07-2022) Exam Date: 29 Oct, 2022 Enrollment Ends: 1 Aug, 2022	

Back to VII Electives

Program: VII Semester Bachelor of Engineering (Electronics & Communication Engineering)		
Course Code: **22EECE430**	Course Title: **Fabrication Techniques for MEMs-based sensors (Swayam)**	
L-T-P: 0-0-3	Credits: 03	Contact Hrs: 03
ISA Marks: 100	ESA Marks: --	Total Marks: 100
Teaching Hrs: 42		Exam Duration: 03hrs

Content	Hours
Prof. Hardik Jeetendra Pandya, IISc Bangalore NPTEL 12 Weeks (Starts: 25-07-2022) Exam Date: 30 Oct, 2022 Enrollment Ends: 1 Aug, 2022	

Back to VII Electives

Program: VII Semester Bachelor of Engineering (Electronics & Communication Engineering)		
Course Code: 22EECE431	Course Title: Cryptography & Network Security (Swayam)	
L-T-P: 0-0-3	Credits: 03	Contact Hrs: 03
ISA Marks: 100	ESA Marks: --	Total Marks: 100
Teaching Hrs: 42		Exam Duration: 03hrs

Content	Hours
Prof. Sourav Mukhopadhyay, IIT Kharagpur NPTEL12 Weeks (Starts: 25-07-2022) Exam Date: 29 Oct, 2022 Enrollment Ends: 1 Aug, 2022	

Back to VII Electives

Program: VII Semester Bachelor of Engineering (Electronics & Communication Engineering)		
Course Code: 22EECE432	Course Title: Phase-locked loops(Swayam)	
L-T-P: 0-0-3	Credits: 03	Contact Hrs: 03
ISA Marks: 100	ESA Marks: --	Total Marks: 100
Teaching Hrs: 42		Exam Duration: 03hrs

Content	Hours
Prof. Saurabh Saxena, IIT Madras NPTEL 12 Weeks (Starts: 25-07-2022) Exam Date: 29 Oct, 2022 Enrollment Ends: 1 Aug, 2022	

Back to VII Electives

Program: VII Semester Bachelor of Engineering (Electronics & Communication Engineering)		
Course Code: 22EECE433	Course Title: Advanced Computer Graphics (IITD + KLE Tech)	
L-T-P: 0-0-3	Credits: 03	Contact Hrs: 03
ISA Marks: 100	ESA Marks: --	Total Marks: 100
Teaching Hrs: 42		Exam Duration: 03hrs

Content	Hours

Advanced Computer Graphics

Subodh Kumar
Professor,
Department of Computer Science and Engineering,
Indian Institute of Technology Delhi.
subodh@cse.iitd.ac.in

#	Topics	Hours
1	Review of Rasterization and Ray tracing	3.0
2	Rendering acceleration data structures	3.0
3	Applications of Texture mapping	3.0
4	Physically based lighting models, global illumination	6.0
5	Multi-pass shading techniques	3.0
6	Surface design and representation (Implicit and Parametric forms)	6.0
7	Mesh Parameterization	3.0
8	Mesh simplification	3.0
9	Animation	6.0
10	Virtual world design	3.0
11	Volume rendering	3.0

Back to VII Electives

Course Code: 22EECE434	Advanced Computer Vision(IITD + KLE Tech)	
L-T-P: 0-0-3	Credits: 03	Contact Hrs: 03
ISA Marks: 100	ESA Marks: --	Total Marks: 100
Teaching Hrs: 42		Exam Duration: 03hrs

Content	Hours

Advanced Computer Vision

Chetan Arora,
Associate Professor,
Department of Computer Science and Engineering,
Indian Institute of Technology Delhi.
chetan@cse.iitd.ac.in

#	Topics	Hours
1	Basics of Machine Learning, and Convolutional Neural Networks	1.5
2	Optimization strategies for training deep neural networks	1.5
3	Advanced Architectures for Image Classification (VGGNet, InceptionNet, ResNet, DenseNet, MobileNets etc.)	3.0
4	Techniques for Visualizing CNNs for Image Analysis	3.0
5	Traditional Techniques for Object Detection (Viola-Jones, Parts based models etc.)	3.0
6	Modern Techniques for Object Detection (Single shot and two shot detectors, keypoint based detectors)	4.5
7	Traditional Techniques for Image Segmentation	3.0
8	Modern Techniques for Image Segmentation	4.5
9	Generating Synthetic Images (AR models, VAEs and GANs)	4.5
10	Vision and Language	4.5
11	Learning Models for Geometrical Vision Problems	3.0
12	Object Tracking	3.0
13	Attack and defense techniques for computer vision systems	3.0

Back to VII Electives