KLE Technological University | Creating Value, Leveraging Knowledge

Curriculum Structure and Curriculum Content for the Academic Batch– 2023-25
School /Department: Electronics & Communication Engineering
Program: Post Graduate in VLSI Design and Embedded Systems

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Vision and Mission

Vision

KLE Tech-School of Electronics and Communication (VLSI Design & Embedded System) will be well recognized nationally and internationally for excellence in its educational programs, pioneering research and impact on the industry and society.

Mission

1. To create a unique learning environment through rigorous curriculum of theory and practice that develops students' technical, scientific and professional skills, and qualities to succeed in wide range of electronics and computing businesses and occupations.
2. To nurture spirit of innovation and state-of-the-art research to advance the boundaries of disciplinary and interdisciplinary knowledge and its applications.
3. To collaborate within and beyond the discipline to create solutions that benefit humanity and society.

Program Educational Objectives (PEO's)

1. Graduates will demonstrate peer- recognized technical competency to solve contemporary problems in the analysis, design and development of electronic devices and systems.
2. Graduates will demonstrate leadership and initiative to advance professional and organizational goals with commitment to ethical standards of profession, teamwork and respect for diverse cultural background.
3. Graduates will be engaged in ongoing learning and professional development through pursuing higher education, and self-study.
4. Graduates will be committed to creative practice of engineering and other professions in a responsible manner contributing to the socio- economic development of the society.

Program Outcomes (PO's)

The graduates will have,

1. An ability to independently carry out research /investigation and development work to solve practical problems.
2. An ability to write and present a substantial technical report/document.
3. Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program.
4. An ability to use modern computational tools in modeling, simulation and analysis pertaining to VLSI Design and Embedded Systems.
5. An ability to work with integrity and ethics in their professional practice, having an understanding of responsibility towards society with sustainable development for lifetime.

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Curriculum Structure-Overall

Semester	Total Program Credits: 88			
	I	II	III	IV
Course with Course Code	Data Structures using C 18EVEC701 0-0-3	Mathematical Thinking and Logical Reasoning 15EHSC701 3-0-0	Internship/ Mini Project 17EVEI801 0-0-8	Project Phase II / Major Project 17EVEW 802 0-0-20
	Analog Circuits 20EVEC702 3-0-0	Automotive Electronics and Communication 19EVEC701 3-0-1		
	CMOS VLSI Design 22EVEC704 3-0-1	Real Time Embedded Systems 19EVEC702 3-0-1		
	Advanced Digital Logic Design 17EVEC710 0-0-2	Advanced Digital Logic Verification 19EVEC703 0-0-3		
	Machine Learning 22EVEC708 3-0-1	Analog & Mixed Mode VLSI Circuits 21EVEC704 3-0-0	Project Phase I / Minor project 17EVEW801 0-0-10	
	RISC Architectures and Programming 17EVEC705 4-0-1	ELECTIVE -1 2-0-1		
	Electronic System Design 17EVEC707 0-0-3	ELECTIVE – 2 2-0-1		
		Mini Project 0-0-3		
Credits	24	26	18	20

Semester: I Semester M. Tech

Program: VLSI Design & Embedded Systems		
Course Title: Data Structures using C		**Course Code: 18EVEC701**
L-T-P: 0-0-3	**Credits: 3**	**Contact Hours: 6 hrs./week**
ISA Marks: 80	**ESA Marks: 20**	**Total Marks: 100**
Teaching Hours: 25	**Examination Duration: 3 hrs.**	

Chapter 01: C language features (05 hrs.)

Pointers revisited, Strings, Structures – Basics, Structures and functions, Arrays of structures, Pointers to structures, Self-Referential Structures, Unions and bit fields, Files.

Chapter 02: Stacks and Queues (05 hrs.)

Definition, Representation and Applications of stack. Definitions, representation and applications of linear, circular, queues, multiple queues, priority queue. Recursion

Chapter 03: Lists (05 hrs.)

Linked lists, singly, doubly, circular lists, definitions, representations. Implementation of list operations, applications – polynomial addition, addition of long integers. Linked stacks, Linked Queues

Chapter 04: Trees (05 hrs.) + (05 hrs.)

Binary trees – Definitions, traversals (recursive and iterative versions), Building and searching, Threaded Binary trees, Trees and their applications

Exchange sorts, Selection and tree sorts, Merge and radix sorts

Text Books

1. Aaron M. Tenenbaum, et al, Data Structures using C, II Edition, PHI, 2006
2. Horowitz, Sahani, Anderson-Feed, Fundamentals of Data Structures in C, II Edition, University, 2008

References

1. E Balaguruswamy, The ANSI C programming Language, II Edition, PHI, 2010
2. Yashavant Kanetkar, Data Structures through C, II Edition, BPB public, 2010

Richard F. Gilberg, Behrouz A. Forouzan , Data Structures: A Pseudocode Approach With C, II Edition, Course Tec, 2009

Lab:

1. Programs on Pointer concepts.
2. Programs on string handling functions, structures union And bit-files.
3. Programming on files
4. Programming on stacks data structures
5. Programs on implementation of different queue data structures.
6. Programs on implementation of different types of Linked lists
7. Programs on Implementation of trees
8. Programs to implement different sorting techniques.
9. Programming on graph
10. Programming on hashing tables
11. Design and implement stack queue data structures
12. Design and implement linked list data structures Project
13. Project

Program: VLSI Design & Embedded Systems		
Course Title: Analog Circuits		**Course Code: 20EVEC702**
L-T-P: 3-0-0	**Credits: 3**	**Contact Hrs.: 5 hrs./week**
ISA Marks: 50	**ESA Marks: 50**	**Total Marks: 100**
Teaching Hrs.: 41	**Exam Duration: 03 hrs.**	

Part - A

Chapter 01: Network Theorems (06 hrs.)

Review of circuit analysis basics: KCL, KVL, Mesh and Nodal analysis. Circuit Analysis Techniques: Linearity and Superposition, Source Transformations, Thevenin's and Norton's Equivalent Circuits, Maximum Power Transfer, Delta-Wye conversion

Chapter 02: First and Second order circuits (04 hrs.)

Order of a system, Concept of Time constant, System Governing equation, System Characteristic equation, Initial conditions, Transfer Functions (Fourier and Laplace domain representation) Frequency and Time response of RLC circuits.

Chapter 03: Two port Networks (04 hrs.)

Admittance, Impedance and Hybrid Parameters. Transmission Parameters

Part - B

Chapter 04: MOS Amplifiers: (06 hrs.)

MOS Structure. The MOS System under external Bias. Structure & Operation of MOS Transistor (MOSFET). MOSFET Current Voltage Characteristics. MOSFET Scaling and Small Geometry Effects. MOSFET Capacitances

Chapter 05: Current Mirrors: (04 hrs.)

Current Mirror circuits and Modeling. Figures of merit (output impedance, voltage swing). Widlar, Cascode and Wilson current Mirrors. Current source and Current sink

Chapter 06: Basic Differential Amplifier Analysis: (05 hrs.)

Basic differential amplifier, Common mode and difference mode gain, CMRR, 5-pack Differential Amplifier with design, Slew rate limitation, Instability and Compensation, Bandwidth and frequency response curve.

Part - C

Chapter 06: Differential Amplifier Design: (12 hrs.)

Design of 5-pack and 7-pack PMOS and NMOS Differential Amplifier, Slew rate limitation, Instability and Compensation, Bandwidth and frequency response curve.

Text books

1. 'William Hayt and Jack Kemmerly and Jamie Phillips and Steven Durbin, "Engineering Circuit Analysis", 9th Edition, Mc Graw Hill publications, 2019
2. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Second edition, Mc Graw Hill publications, 2017
3. Phillip E. Allen, Douglas R. Holberg, "CMOS Analog Circuit Design", Oxford University Press, USA; 3rd Revised ed. edition (July 1, 2012)

References books

1. Behzad Razavi, "Fundamentals of Microelectronics", Second edition, John Wiley & Sons (April 2013)
2. Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G. Meyer, "Analysis and design of Analog Integrated Circuits",5th edition, John Wiley & Sons (January 2009)
3. Adel S. Sedra and Kenneth C. Smith, "Microelectronic Circuits", 7E, Oxford University Press (2015)
4. R. Jacob Baker, "CMOS Circuit Design, Layout, and Simulation", 3rd edition, John Wiley & Sons (2010)

Program: VLSI Design & Embedded Systems		
Course Title: CMOS VLSI Design		Course Code: 22EVEC704
L-T-P: 3-0-1	Credits: 4	Contact Hours: 5 Hrs./week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 52 Hrs.	Examination Duration: 3 hrs.	

Chapter 01. Introduction to VLSI and IC fabrication technology (10 hrs.)

VLSI Design Flow, MOS theory, Introduction, nMOS / pMOS enhancement transistors, Comparison of BJTs and MOSFETs, Threshold voltage equation, MOS device design equations, MOS capacitance models, Second order effects: Sub-threshold conduction, Velocity Saturation and Mobility Degradation, Channel length modulation, Body Effect, Junction Leakage, Tunneling, Temperature Dependence. FinFET device, The root cause of short channel effects in twenty-first century MOSFETS, The thin body MOSFET concept, The FinFET and a new scaling path for MOSFETs, Ultra thin body FET.

Chapter 02 IC fabrication technology (12 hrs.)

Semiconductor Technology - An Overview, Czochralski method of growing Silicon,Wafer cleaning process, Introduction to Unit Processes (Oxidation, Diffusion, Deposition, Ion-implantation), Basic CMOS technology - Silicon gate process, n-Well process, p-Well process, Twin-tub Process.

Chapter 03. DC Analysis of CMOS logic gates (04 hrs.)

DC transfer characteristics of CMOS inverter, Beta Ratio Effects, Noise Margin, MOS capacitance models.

Chapter 04. Transient Analysis of CMOS logic gates (06 hrs.)

Transient Analysis of CMOS Inverter, NAND, NOR and Complex Logic Gates, Gate Design for Transient Performance, Switch-level RC Delay Models, Delay Estimation, Elmore Delay Model, Power Dissipation of CMOS Inverter, Transmission Gates & Pass Transistors, Tristate Inverter.

Chapter 05. Designing High-Speed CMOS Logic Networks (10 hrs.)

Stick Diagrams, Euler Path, Layout design rules, DRC, Circuit extraction, Latch up –
Triggering Prevention, Gate Delays, Driving Large Capacitive Loads, Delay Minimization in an Inverter Cascade, Logical effort, BiCMOS Drivers.

Chapter 06. Combinational CMOS Circuit Design (05 hrs.)

Pseudo nMOS, Clocked CMOS, Dynamic CMOS Logic Circuits, Dual-rail Logic Networks: CVSL, CPL.

Chapter 07. Sequential CMOS Circuit Design (05 hrs.)

Sequencing static circuits, Circuit design of latches and flip-flops, Clocking- clock generation, clock distribution.

Text Books

1. John P. Uyemura, Introduction to VLSI Circuits and Systems, 1, Wiley, 2007
2. Neil Weste, David Harris & Ayan Banerjee, CMOS VLSI Design, 3, Pearson Ed, 2005
3. Sung-Mo Kang & Yusuf Leblebici, CMOS Digital Integrated Circuits: Analysis and Design, 3, Tata McGraw, 2007
4. Sorab K. Ghandhi, VLSI Fabrication Principles, Wiley, 2nd edition, 1994

References

1. FinFET Modeling for IC Simulation and Design: Using the BSIM-CMG Standard
By Yogesh Singh Chauhan, Darsen Duane Lu, Vanugopalan Sriramkumar, Sourabh Khandelwal, Juan Pablo Duarte,
Navid Payvadosi, Ai Niknejad, Chenming Hu, Elsevier Publication, 2015
2. Wayne, Wolf, Modern VLSI design: System on Silicon, 3, Pearson Ed, 2005
3. Douglas A Pucknell and Kamran Eshraghian, Basic VLSI Design, 3, PHI, 2005
4. Phillip. E. Allen, Douglas R. Holberg, CMOS Analog circuit Design, 1, Oxford Uni, 2002

Lab:

1. Introduction to Cadence EDA tool.
2. Static and Dynamic Characteristic of CMOS inverter.
3. Layout of CMOS Inverter (DRC,LVS)
4. Static and Dynamic Characteristic of CMOS NAND2 and NOR2
5. Layout of NAND2, NOR2, XOR2 gates (DRC, LVS).
6. Design a Phase Detector using D-FF
7. Design complex combinational circuits and analyze the performance using Cadence tool.

Program: VLSI Design and Embedded System		
Course Title: Advanced Digital Logic Design		Course Code: 17EVEC710
L-T-P: 0-0-2	Credits: 2	Contact Hours: 4Hrs/week
ISA Marks: 100	SEE Marks:	Total Marks: 100
Teaching Hrs.: 50 hrs.	Examination Duration:	

Chapter 01. Digital Integrated Circuits (10 hrs.)

Moore's law, Technology Scaling, Die size growth, Frequency, Power dissipation, Challenges in digital design, Design metrics, Cost of Integrated circuits, ASIC , Evolution of SoC ASIC Flow Vs SoC Flow, SoC Design Challenges. Introduction to CMOS Technology, PMOS & NMOS Operation, CMOS Operation principles, Characteristic curves of CMOS, CMOS Inverter and characteristic curves, Delays in inverters, Buffer Design, Power dissipation in CMOS, CMOS Logic, Stick diagrams and Layout diagrams. Setup time, Hold Time, Timing Concepts

Chapter 02. Digital Building Blocks (10 hrs.)

Basic Gates, Universal Gates, nand & nor Implementations. Decoder, encoder, code converters, Priority encoder, multiplexer, demultiplexer, Comparators, Parity check schemes, Multiplexer, De-multiplexer, Pass Transistor Logic, application of multiplexer as a multi-purpose logical element. Asynchronous and synchronous up-down counters, Shift registers. FSM Design, Mealy and Moore Modelling, Adder & Multiplier concepts, Memory Concept

Chapter 03. Logic Design Using Verilog (12 hrs.)

Evolution & importance of HDL, Introduction to Verilog, Levels of Abstraction, Typical Design Flow, Lexical Conventions, Data Types Modules, Nets, Values, Data Types, Comments, arrays in Verilog, Expressions, Operators, Operands, Arrays, memories, Strings , Delays , parameterized designs Procedural blocks, Blocking and Non-Blocking Assignment, looping, flow Control, Task, Function, Synchronization, Event Simulation. Need for Verification, Basic test bench generation and Simulation

Chapter 04. Principles of RTL Design (08 hrs)

Verilog Coding Concepts, Verilog coding guide lines: Combinational, Sequential, FSM. General Guidelines, Synthesizable Verilog Constructs, Sensitivity List, Verilog Events, RTL Design Challenges, Clock Domain Crossing. Verilog modelling of combinational logic and sequential logic

Chapter No. 5. Design and simulation of Architectural building blocks (10 hrs)

Basic Building blocks design using Verilog HDL: Arithmetic Components – Adder, Subtractor, and Multiplier design, Data Integrity – Parity Generation circuits, Control logic – Arbitration, FSM Design – overlapping and non-overlapping Mealy and Moore state machine design

Reference Books:

1. Digital Design by Morris Mano M, 4th Edition.
2. Verilog HDL: A Guide to Digital Design and Synthesis by Samir Palnitkar, 2nd Edition
3. Principles of VLSI RTL Design: A Practical Guide by Sapan Garg, 2011 Tools: 1. NC Verilog, NC Sim, CVER + GTKWave, VCSMX, Modelsim for Verilog 2. Microwind for layout.

Program: VLSI Design and Embedded System		
Course Title: Machine Learning		**Course Code: 22EVEC708**
L-T-P: 3-0-1	**Credits: 4**	**Contact Hours: 5Hrs/week**
ISA Marks: 50	**SEE Marks: 50**	**Total Marks: 100**
Teaching Hrs.: 40 hrs.	**Examination Duration: 3 hrs.**	

Chapter 01. Introduction (05 hrs.)

Introduction What is Machine Learning? Applications of Machine Learning, Types of Machine Learning: Supervised, Unsupervised and Reinforcement learning, Dataset formats, Basic terminologies

Chapter 02. Supervised Learning (10 hrs.)

Linear Regression, Logistic Regression Linear Regression: Single and Multiple variables, Sum of squares error function, The Gradient descent algorithm, Application, Logistic Regression, The cost function, Classification using logistic regression, one-vs-all classification using logistic regression, Regularization.

Chapter 03. Supervised Learning: Neural Network (10 hrs.)

Introduction to perception learning, implementing simple gates XOR, AND, OR using neural network. Model representation, Gradient checking, Back propagation algorithm, multi-class classification, Application- classifying digits, SVM.

Chapter 04. Unsupervised Learning: Clustering (05 hrs.)

Introduction, K means Clustering, Algorithm, Cost function, Application

Chapter 05. Unsupervised Learning: Dimensionality Reduction (05 hrs.)

Dimensionality reduction, PCA- Principal Component Analysis. Applications, Clustering data and PCA

Chapter 06. Machine Learning System Design (05 hrs.)

Evaluating a hypothesis, Model selection, Bias and variance, error analysis, error metrics for skewed classes. Building a Model.

Text Books:

1. Tom Mitchell, Machine Learning, 1, McGraw-Hill. , 1997
2. Christopher Bishop, Pattern Recognition and Machine Learning, 1, Springer, 2007

Reference Books:

1. Video lectures by : Andrew Ng, Co-founder, Coursera; Adjunct Professor, Stanford University; formerly head of Baidu AI Group/Google Brain https://www.coursera.org/learn/machine-learning#

2. Trevor Hastie, Robert Tibshirani, Jerome Friedman, The Elements of Statistical Learning: Data Mining, Inference and Prediction, 2, Springer, 2009

Implementation Assignments:

1. Assignments are designed to explore the concepts like
   - Supervise and unsupervised learning,
   - Clustering,
   - Regression and estimation
2. Motivate students to take up open challenges like Kaggle, walmart, ect
3. To explore different Machine Learning Tools/ Libraries.

Program: VLSI Design and Embedded System		
Course Title: RISC Architectures and Programming		Course Code: 17EVEC705
L-T-P: 4-0-1	Credits: 5	Contact Hours: 6Hrs/week
ISA Marks: 50	SEE Marks:50	Total Marks: 100
Teaching Hrs.: 50 hrs.	Examination Duration:3Hrs	

Chapter 01. The 32-bit RISC Architecture (06 hrs.)

The Acorn RISC machine, Architectural inheritance, Architecture of ARM7TDMI, ARM programmers' model, ARM development tools, 3 stage pipeline ARM organization, ARM instruction execution.

Chapter 02. Instruction sets, Assembly and Embedded C Programming (06 hrs.)

Features of ARM Instruction, Data processing instruction, Branch/Control instruction and Data Transfer/Load store instruction. Software interrupt instruction, Program status register instruction, Conditional execution, Example programs, 16bit Instruction set-The Thumb programmer model, ARM-Thumb interworking, Thumb branch instructions, Data processing instructions, Single/Multiple register load store instruction, Stack operation, Software interrupt instructions, example programs.

Chapter 03. Introduction to LPC2148 and Embedded C programming (04 hrs.)

Architectural Overview of LPC2148, Features and Memory mapping of LPC2148, Interfacing of Basics peripherals to LPC2148 and programming using Embedded C.

Chapter 04. Exception Handling (04 hrs.)

Introduction, Interrupts, error conditions, processor exception sequence, the vector table, Exception handlers, Exception priorities, Procedures for handling exceptions.

Chapter 05. Memory Hierarchy Design (06 hrs.)

Cache basics, Miss rate and penalty, Cache Hierarchy, Memory Organizations, Memory Hierarchy.

Chapter 06. Pipelining (08 hrs.)

Linear pipeline processor, Nonlinear pipeline processor, Instruction pipeline design, Branch handling techniques, Arithmetic pipeline design, Computer arithmetic principles, Static arithmetic pipeline, Multifunctional arithmetic pipeline

Chapter 07. Cortex M4 (06 hrs.)

Functional description, programmer's model, memory protection unit, nested vectored interrupt controller.

Chapter 08. Multi-Core Architectures (07 hrs.)

Introduction to Intel Architecture, How an Intel Architecture System works, Basic Components of the Intel Core 2 Duo Processor: The CPU, Memory Controller, I/O Controller.

Chapter 09. Current Trends in Intel Architectures and Applications (03 hrs.)

Seminar on current trends in Intel Architectures

Reference Books:

1. ARM System- on-Chip Architecture" by 'Steve Furber', LPE, Second Edition.
2. "ARM Assembly Language fundamentals and Techniques" by William Hohl, CRC press, 2009.
3. D. A. Patterson and J. L. Hennessey "Computer Organization and Design", Morgan, Kaufmann,2002
4. H. Jonathan Chao and Bin Liu, "High performance switches & routers", Wiley Interscience, 2007.
5. Kai Hwang, "Advanced Computer Architecture – TMH – 1993
6. Web resources for Example Architectures of INTEL and Texas Instruments:
   http:/ /download.intel.com/design/intarch/papers/321087.pdf

References

1. Kai Hwang, Faye A. Briggs, Computers Architecture and Parallel Processing – MGH – 1985
2. David E Culler, Jaswinder Pal Singh, Anoop Gupta "Parallel Computer Architecture", Harcourt Asia Pte Ltd 2000
3. Stalling W." Computer Organization and Architecture- Designing for performance" PHI,2005
4. D. Sima,T. Fountain, P.Kasuk," Advanced Computer Architecture-A Design Space Approach" Addisson Wesley,1997.
5. M. J. Flynn,"Computer Architecture, Pipelined And Parallel Processing", Narosa Publications, 1998.

List of Experiments:

1. Write an ALP to verify data transfer w.r.t memory to achieve following,
   i. 8-bit data transfer and exchange
   ii. 16-bit data transfer and exchange
   iii. 32-bit data transfer and exchange
2. Write an ALP for Tables and lists to do following,
   i. Add an entry to a list
   ii. Remove an element from the queue
3. Write an ALP to pass parameters to a subroutine,
   i. Ascending order
   ii. Descending order
4. Write an ALP for following,
   i. Finding length of a string
   ii. Compare two strings for equality
   iii. To find whether given string is palindrome
5. Write a 'C' program & demonstrate an interfacing of Alphanumeric LCD 2X16 panel to LPC2148Microcontroller
6. Write a 'C' program & demonstrate an interfacing of Seven segment to LPC2148 Microcontroller.
7. Write a 'C' program & demonstrate an interfacing of UART to LPC2148 Microcontroller.
8. Write a 'C' program & demonstrate an interfacing of ADC to LPC2148 Microcontroller.
9. Write a 'C' program & demonstrate an interfacing of Keypad to LPC2148
10. Write a 'C' program & demonstrate interface DAC to LPC2148
11. Develop a code for electronic voting machine.

Reference Books

1. "ARM System- on-Chip Architecture" by 'Steve Furber", LPE, Second Edition.
2. "Embedded Systems- Architecture, Programming and Design" by Raj Kamal, TMH
3. Dr. K.V.K.K. Prasad, "Embedded/Real-time systems: concepts, Design & Programming", published by dreamtech press.

Manual

1. LPC2148 datasheet by NXP.

2. LPC2148 board manual by ALS, Bangalore

Program: VLSI Design and Embedded System		
Course Title: Electronic System Design		**Course Code: 17EVEC707**
L-T-P: 0-0-3	**Credits: 3**	**Contact Hours: 6Hrs/week**
ISA Marks: 100	**SEE Marks:**	**Total Marks: 100**
Teaching Hrs.: 25 hrs.	**Examination Duration:3Hrs**	
To level specifications, Block level specifications, Timing of micro architecture, Verification and test plan, Schematic capture (05 hrs.)		
Simulation, Advanced simulation, Signal Integrity (05 hrs.)		
PCB layout- Floor planning, component pre planning, PCB printing- 2 layer (05 hrs.)		
Functionality and performance check, Failure analysis, Validation and system integration (05 hrs.)		
System Analysis (05 hrs.)		

References

1. A. S Sedra and KC Smith, Microelectronic circuits, Oxford, 1998.
2. G.L. Ginsberg, Printed Circuit Design, McGraw Hill, 1991

Semester: II Semester M. Tech		
Course Title: Mathematical Thinking and Logical Reasoning		Course Code: 15EHSC701
L-T-P: 3-0-0	Credits: 3	Contact Hours: 3Hrs/week
ISA Marks: 50	SEE Marks: 50	Total Marks: 100
Teaching Hrs.: 40 hrs.	Examination Duration: 3 hrs.	

1. **Quantitative Aptitude (10hrs.)**
2. **Analytical Puzzles (04 hrs.)**
3. **Syllogistic Logic (03 hrs.)**
4. **Verbal Reasoning (09 hrs.)**
5. **Visual Reasoning (06 hrs.)**
6. **Advanced Lateral Thinking (08 hrs.)**

Text Books

1. A Modern Approach to Verbal and Non – Verbal Reasoning – R. S. Aggarwal, Sultan Chand and Sons, New Delhi.
2. Quantitative Aptitude – R. S. Aggarwal, Sultan Chand and Sons, New Delhi.

Reference Books:

1. Verbal and Non – Verbal Reasoning – Dr. Ravi Chopra, MacMillan India
2. Lateral Thinking – Dr. Edward De Bono, Penguin Books, New Delhi

Program: VLSI Design & Embedded Systems		
Course Title: Automotive Electronics and Communication		Course Code: 19EVEC701
L-T-P: 3-0-1	Credits: 4	Contact Hours: 5 hrs./week.
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 50	Examination Duration: 3 hrs.	

Chapter No: 1. Automotive Systems, Design cycle and Automotive industry overview (09 Hrs.)

Overview of Automotive industry, Vehicle functional domains and their requirements, automotive supply chain, global challenges. Role of technology in Automotive Electronics and interdisciplinary design. Introduction to modern automotive systems and need for electronics in automobiles and application areas of electronic systems in modern automobiles, Introduction to power train, Automotive transmissions system, Vehicle braking fundamentals, Steering Control, Overview of Hybrid Vehicles, ECU Design Cycle: Types of model development cycles(V and A) , Components of ECU, Examples of ECU on Chassis, Infotainment, Body Electronics and cluster.

Chapter No: 2. Embedded system in Automotive Applications & Automotive safety systems (10 Hrs.)

Automotive grade microcontrollers: Architectural attributes relevant to automotive applications, Automotive grade processors ex: Renesas, Quorivva, and Infineon. EMS: Engine control functions, Fuel control, Electronic systems in Engines , Development of control algorithm for EMS, Look-up tables and maps, Need of maps, Procedure to generate maps, Fuel maps/tables, Ignition maps/tables, Engine calibration, Torque table, Dynamometer testing Safety Systems in Automobiles: Active and Passive safety systems: ABS, TCS, ESP, Brake assist, Airbag systems etc.

Chapter No: 3. Automotive Sensors and Actuators (09 Hrs.)

Sensor characteristics, Sensor response, Sensor error, Redundancy of sensors in ECUs, Avoiding redundancy, Smart Nodes, Examples of sensors: Accelerometer (knock sensors),wheel speed sensors, Engine speed sensor, Vehicle speed sensor, Throttle position sensor, Temperature sensor, Mass air flow (MAF) rate sensor, Exhaust gas oxygen concentration sensor, Throttle plate angular position sensor, Crankshaft angular position/RPM sensor, Manifold Absolute Pressure (MAP) sensor. Actuators: Engine Control Actuators, Solenoid actuator, Exhaust Gas Recirculation Actuator.

Chapter No: 4. Automotive communication protocols (10 Hrs.)

Overview of Automotive communication protocols : need for communication in Automotive, overview of vehicle network architecture, need for CAN in Automotive, CAN Bus logic ,CAN frame formats, CAN bus fault confinement, LIN , Flex Ray, MOST.

Chapter No: 5. Advanced Driver Assistance Systems (ADAS) and Functional safety standards (07 Hrs.)

Advanced Driver Assistance Systems (ADAS): Examples of assistance applications: Lane Departure Warning, Collision Warning, Automatic Cruise Control, Pedestrian Protection, Headlights Control, Connected Cars technology and trends towards Autonomous vehicles. Functional Safety: Need for safety standard-ISO 26262, safety concept, safety process for product life cycle, safety by design, validation.

Chapter No: 6. Diagnostics (05 Hrs.)

Fundamentals of Diagnostics: Basic wiring system and Multiplex wiring system, Preliminary checks and adjustments, Self-diagnostic system. Fault finding and corrective measures, Electronic transmission checks and Diagnosis, Diagnostic procedures and sequence, On board and off board diagnostics in Automobiles, OBDII,

Concept of DTCs, DLC, MIL, Freeze Frames, History memory, Diagnostic tools, Diagnostic protocols: KWP2000 and UDS.

Text books:

1. William B. Ribbens, Understanding Automotive Electronics, 6, Newnes Publications, 2003
2. Denton.T , Automobile Electrical and Electronic Systems, Edward Arnold , 1995

References:

1. William T.M , Automotive Electronic Systems, Heiemann Ltd., London , 1978
2. Nicholas Navet , Automotive Embedded System Handbook, CRC Press , 2009

Lab:

1. Demonstration of cut section modules: Engine, Transmission , Steering, Braking, Suspension - Automobile dept.
2. Electronic engine control system: Injection and Ignition control system Transmission trainer modules
3. Modeling an engine Vehicle model simulation with Simulink using PI CONTROLLER
4. Basic gate logic simulation and modeling using Simulink and realization on the hardware platform.
5. Seat belt warning system simulation and modeling using Simulink and realization on the hardware platform. Vehicle speed control based on the gear input simulation and modeling using Simulink and realization on the hardware platform.
6. Throttle control modeling and simulation using Simulink and realization on the hardware platform.
7. Accelerator pedal interfacing software modeling and simulation using Simulink and realization on the hardware platform.
8. Develop matlab code for stepper motor control and convert it to Simulink model and port it to embedded hardware

Program: VLSI Design & Embedded Systems		
Course Title: Real Time Embedded System		**Course Code: 19EVEC702**
L-T-P: 3-0-1	**Credits: 4**	**Contact Hours: 5 Hrs./week**
ISA Marks: 50	**ESA Marks: 50**	**Total Marks: 100**
Teaching Hours: 45 Hrs.	**Examination Duration: 3 hrs.**	

Chapter 01. Building blocks: (12 hrs.)

Real Time System, Types, Real Time Computing, Design Issue, Sample Systems, Hardware Requirements- Processor in a system, System Memories, System I/O, De-bouncing, Other Hardware Devices (A/D, D/A, USART, Watchdog Timers, Interrupt Controllers). Device Drivers, Interrupt Servicing Mechanism & Interrupt Latency.

Chapter 02. Advanced Processors: (10 hrs.)

Automotive Grade Processors: AEC-Q100 qualification, Qorivva 32-bit Microcontrollers, MPC577XK for ADAS, AURIX from Infineon, Tricore Architecture, Renasas RL78/D1x (Automotive Only)

Chapter 03. Real Time Operating System: (04 hrs.)

Interrupt driven systems, foreground/background systems, full featured rtos, POSIX, buffering data, mailboxes, critical regions, semaphores, event flags & signals, deadlock, process stack management, dynamic allocation.

Chapter 04. Case Studies: (06 hrs.)

Mucos/ VX Works Functions – System level, task service, time delay, memory allocation, semaphore, mailbox, queue.

Example systems: Coding for Automatic chocolate vending machine using MUCOS & Coding for sending application layer byte streams on a TCP/IP Network using Vx Works.

Chapter 05. Process of Embedded System Development: (08 hrs.)

Development process, requirements engineering, design, implementation, integration & testing, packaging, configuration management, managing embedded system development, embedded system fiascos.

Chapter 06. Current trends, ethical & environmental issues (05 hrs.)

The students shall give seminars on current trends in the field of RTES, ethical, & environmental issues.

Text Books

1. Philip. A. Laplante, "Real-Time Systems Design and Analysis- an Engineer's Handbook"- Second Edition, PHI Publications.
2. Rajkamal, "Embedded Systems: Architecture, Programming and Design", Tata McGraw Hill, New Delhi, 2003.
3. Dr. K.V.K K Prasad, "Embedded Real Time Systems: Concepts Design and Programming", Dreamtech Press New Delhi, 2003.

References

1. Joseph Yiu, "The Definitive guide to ARM CORTEX –M3 & CORTEX-M4 Processors", Elsevier, Newnes, 2014.
2. Steve Furber "ARM System –on – Chip Architecture" Second Edition, Pearson Education
3. David E. Simon, "An Embedded software primer", Pearson Education, 1999..
4. David A. Evesham, "Developing real time systems – A practical introduction", Galgotia Publications, 1990
5. William Hohl, "ARM Assembly Language Fundamentals & Techniques", CRC Press
6. C. M. Krishna, "Real Time Systems" MGH, 1997
7. Jane W.S. Liu, "Real-Time Systems", Pearson Education Inc., 2000

Program: VLSI Design & Embedded Systems		
Course Title: Advanced Digital Logic Verification		**Course Code: 19EVEC703**
L-T-P: 0-0-3	**Credits: 3**	**Contact Hours: 6 Hrs./week**
ISA Marks: 50	**ESA Marks: 50**	**Total Marks: 100**
Teaching Hours: 50 Hrs.	**Examination Duration: 3 hrs.**	

Chapter 01. Verification concepts: (10 hrs.)

Concepts of verification, importance of verification, Stimulus vs Verification, functional verification, test bench generation, functional verification approaches, typical verification flow, stimulus generation, direct testing, Coverage: Code and Functional coverage, coverage plan.

Chapter 02. System Verilog – Language Constructs: (10 hrs.)

System Verilog constructs - Data types: two-state data, strings, arrays: queues, dynamic and associative arrays, Structs, enumerated types. Program blocks, module, interfaces, clocking blocks, modports.

Chapter 03. System Verilog – Classes & Randomization: (12 hrs.)

SV Classes: Language evolution, Classes and objects, Class Variables and Methods, Class instantiation, Inheritance, and encapsulation, Polymorphism. Randomization: Directed Vs Random Testing. Randomization: Constraint Driven Randomization.

Chapter No. 4. System Verilog – Assertions & Coverage (08 hrs.)

Assertions: Introduction to Assertion based verification, Immediate and concurrent assertions. Coverage driven verification: Motivation, Types of coverage, Cover Group, Cover Point, Cross Coverage, Concepts of Binning and event sampling.

Chapter 05. Building Testbench: (10 hrs.)

Layered testbench architecture. Introduction to Universal Verification Methodology, Overview of UVM Base Classes and simulation phases in UVM and UVM macros. Unified messaging in UVM, UVM environment structure, Connecting DUT- Virtual Interface

References:

1. System Verilog LRM
2. Chris Spear, Gregory J Tumbush – System Verilog for verification - a guide to learning the testbench language features - Springer, 2012
3. Step-by-Step Functional Verification with System Verilog and OVM by Sasan Iman SiMantis Inc. Santa Clara, CA Spring 2008 Tools: 1. NC Verilog, NC Sim, VCSMX for System.

Program: VLSI Design & Embedded Systems		
Course Title: Analog and Mixed mode VLSI Circuits		**Course Code: 21EVEC704**
L-T-P: 3-0-0	**Credits: 3**	**Contact Hours: 3 hrs./week**
ISA Marks: 50	**ESA Marks: 50**	**Total Marks: 100**
Teaching Hours: 40	**Examination Duration: 3 hours**	

Chapter 01: (06 hrs.)

Basic Current reference, and Voltage (Bandgap) reference circuits, OPAMP based references, Current mode bandgap reference

Chapter 02: (03 hrs.)

Bidirectional analog switch, Sample and Hold circuit, Basic Comparator architecture, non-idealities (offset error, bandwidth consideration), Dynamic comparator, Sense amplifier .

Chapter 03: (07 hrs.)

DAC architecture, Weighted Resistor and R-2R network, their Limitations, Current source-based DAC

Chapter 04: (10 hrs.)

ADC basics, Flash ADC, Tracking ADC, Dual slope ADC, SAR ADC, and their applications

Chapter 05: (06 hrs.)

Pipeline ADC architecture, algorithm and Sigma-Delta ADC

Chapter 06: (08 hrs.)

PLL-operating principles, Phase detector and VCO; Phase frequency Detector, Charge pump models, stability issues, Jitter in PLL.

Text Books

1. Phillip. E. Allen, Douglas R. Holberg, “CMOS Analog circuit Design” Oxford University Press, 2002.
2. Baker, Li, Boyce, “CMOS: Circuit Design, Layout and Simulation”, Prentice Hall of India, 2000

Reference Books

1. N. Weste and K. Eshranghian, Principles of CMOS VLSI Design, Addison Wesley. 1985.
2. J. Rabaey, Digital Integrated Circuits: A Design Perspective, Prentice Hall India, 1997
3. C. Mead and L. Conway, Introduction to VLSI Systems, Addison Wesley, 1979.
4. B Razavi ‘Design of Analog CMOS Integrated Circuits’ First Edition McGraw Hill 2001

Program: VLSI Design & Embedded Systems		
Course Title: Image and Video Processing		Course Code: 17EVEE701
L-T-P: 2-0-1	Credits: 3	Contact Hours: 4 hrs./week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 40	Examination Duration: 3 hours	

Chapter 01: Introduction (02 hrs.)

2D systems, Mathematical Preliminaries- FT, Z-transform, Optical and Modulation Transfer Functions (OTF and MTF). Matrix theory, Image perception: Light, Luminance, Brightness, Contrast, MTF of the visual system, Visibility function, Monochrome Vision Models, Fidelity criteria, Color Representation, Color Vision Models, Temporal Properties of Vision.

Chapter 02: Image sampling and Quantization (02 hrs.)

2D Sampling theory, Quantization, Optimal Quantizer, Compander and Visual Quantization

Chapter 03: Image Transforms (04 hrs.)

2D orthogonal and unitary transforms, DFT, DCT, Harr, KLT

Chapter 04: Image Enhancement (04 hrs.)

Histograms Modeling, Spatial operations, Transform operations, Multispectral Image Enhancement

Chapter 05: Image Filtering and Restoration (04 hrs.)

Image Observation Models, Inverse and Weiner filtering, Frequency Domain Filters. Smoothing Splines and Interpolation.

Chapter 06: Basics of Video: (02 hrs.)

Analog Video, Digital Video

Chapter 07: Two-dimensional motion estimation (07 hrs.)

Optical flow methods**,** Block based methods, Bayesian methods**.**

Text Books

1. Jain, A.K., Fundamentals of Digital Image Processing, 3rd Edision, Pearson Education (Asia) 2013
2. A. Murat Tekalp, Digital Video processing Pearson Education (Asia) Pte. Ltd.
3. Li and, Z. Drew, M.S. Fundamentals of Multimedia, Pearson Education (Asia) Pte. Ltd,. 2010.

Reference Books

1. Gonzalez, Rafael C., Woods, Richard E. and Eddins Steven L., Digital Image Processing Using Matlab, Pearson Education (Asia) Pvt. Ltd.,
2. Al. Bovik, Essential guide to Video Processing, Academic Press

Implementation:

Implementation assignments are designed using OpenCV/C++ to explore the concepts like

1. Image enhancement techniques

2. Image transforms
3. Image restoration technique
4. Develop an image processing application to assist
    a. ADAS
    b. Agriculture
    c. Defense
    d. Health Care
    e. Surveillance and Forensics
    f. Remote sensing
5. Track an object in video
6. Optimal use of surveillance video

Course Title: MEMS	Course code: 19EVEE701	
L-T- P: 2-0-1	Credits: 03	Contact Hrs.: 04hrs/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hrs.: 40	Exam Duration: 3 hrs.	

Chapter 1: Overview of MEMS and Microsystems (05 hrs.)

Evolution of Microsystems, Miniaturization, Applications, Working principles of Microsystems: Introduction to Micro-sensors, Micro-actuation, Example of MEMS with Micro-actuators – Airbag

Chapter 2: Micro-fabrication (10 hrs.)

Different structures used for MEMS devices (combination of Mechanical, electrical), How to create these structures

Materials for MEMS and Microsystems: Silicon as a preferred material, Silicon compounds, GaAS, Quartz, Polymers, piezo-resistors; Machining processes (Bulk, Surface and LIGA processes). Unit processes in VLSI, Oxidation, Diffusion, Deposition, Etching, Photolithography

Chapter 3: Sensing Techniques and Examples (10 hrs.)

PZR, PZE, and Capacitive sensing techniques, Modeling, Design and Analysis with example for each technique. Numerical problem for each technique**.**

Case studies – MEMS resonator, PZR accelerometer (Commercial) **(05 hrs.)**

Chapter 4: Scaling laws in miniaturization: **(04 hrs.)**

Introduction to scaling, scaling in geometry, electrostatic forces, EM forces, Electricity, Numerical problems.

Chapter 5: Modeling: Modeling techniques (06 hrs.)

Mathematical modeling, Electrical modeling (Lumped modeling), Mechanical Modeling, MEMS CAD tools. MEMS as Inductor, Capacitor, Micro-Characterization**.**

Text Book / Reference:

"MEMS and Microsystems – Design and Manufacture", Tai-Ran Hsu, TMH Edition

References:

Micro system Design , Stephen D. Senturia, Kluwer Academic Publishers, 2001.

Program: VLSI Design & Embedded Systems		
Course Title: System on Chip		Course Code: 19EVEE702
L-T-P: 2-0-1	Credits: 3	Contact Hours: 4 hrs./week
CIE Marks: 50	SEE Marks: 50	Total Marks: 100
Teaching Hours: 50	Examination Duration: 3 hours	

Chapter 1: Verification and Technology Options (10 hrs.)

Overview of verification, challenges in verification of SOC, Simulation technologies, Static technologies, Formal technologies, Physical verification and analysis, comparing verification options.

Chapter 2: Verification Methodology: (10 hrs.)

Verification plans, Testbench creation, Testbench migration, Verification languages, Verification device test, System level verification, Verification IP Reuse, Verification approaches.

Chapter 3: System level Verification: (10 hrs.)

System design, System verification, Applying the system level testbench, System testbench migration, Bluetooth SOC.

Chapter 4: Static Netlist Verification: (10 hrs.)

Netlist verification, Bluetooth SOC arbiter, Equivalence checking, Equivalence checking methodology, RTL to RTL verification, RTL to Gate level netlist verification, Gate level netlist to Gate level, Static timing verification and analysis**.**

Chapter 5: SOC Testing (10 hrs.):

Importance of system on chip testing, SOC test issues, FPGA Testing: Overview of FPGA, Testing approaches, BIST of programmable resources, Embedded processor-based testing**.**

Text Books

1. Prakash Rashinkar, Peter Paterson, Leena Singh, " SOC Verification –Methodology and Techniques", Springer 2000
2. Laung-Terng Wang, Charles E. Stroud, Nur A. Touba, "System-on-chip Test Architectures", 2008.

Reference books

1. J-M. Berge, O. Levia, J. Rouillard: Hardware/Software Co-Design and Co-Verification, Kluwer, 1997.
2. M. L. Bushnell and V. D. Agrawal, Essential of Electronics Testing for Digital, Memory and Mixed-Signal Circuits, Kluwer Academic Publishers, 2001.
3. Thomas Kropf, "Introduction to Formal Hardware Verification", Springer 1999.

Program: VLSI Design & Embedded Systems		
Course Title: CMOS ASIC Design		**Course Code: 19EVEE703**
L-T-P: 2-0-1	**Credits: 3**	**Contact Hrs.: 4 hrs./week**
ISA Marks: 50	**ESA Marks: 50**	**Total Marks: 100**
Teaching Hrs.: 24	**Exam Duration: 3 hrs.**	

Chapter No. 1. Introduction to ASIC (04 hrs.)

ASIC types, design flow, economics of ASIC

Chapter No. 2. ASIC design library and Logic cell (05 hrs.)

Transistor as register, transistor parasitic capacitance, Logic Effort, Data Path Elements, Adders, Multiplier, Sequential logic cells, I/O cell.

Chapter No. 3. Logic Synthesis and Simulation (05 hrs.)

Logic synthesis, FSM synthesis, structural simulation, static timing analysis, delay models

Chapter No. 4. ASIC Construction Floor planning and placement and routing (05 hrs)

Physical Design, System Partitioning, Estimating ASIC size, partitioning methods.

Chapter No. 5. Floor planning and placement and routing (05 hrs)

Floor planning tools, I/O and power planning, clock planning, placement algorithms, iterative placement improvement, Time driven placement methods. Physical Design flow global Routing, Local Routing, Detail Routing, Special Routing, Circuit Extraction and DRC.

Text Books:

1. M.J.S .Smith, - “Application - Specific Integrated Circuits” – Pearson Education, 2003.
2. Randall L Geiger, Phillip E. Allen, “Noel K.Strader, VLSI Design Techniques for Analog and Digital Circuits”, McGraw Hill International Company, 1990.

References:

1. Jose E.France, Yannis Tsividis, “Design of Analog-Digital VLSI Circuits for Telecommunication and signal processing”, Prentice Hall, 1994.
2. Andrew Brown, - “VLSI Circuits and Systems in Silicon”, McGraw Hill, 1991.
3. S.D. Brown, R.J. Francis, J. Rox, Z.G. Uranesic, “Field Programmable Gate Arrays”- Kluwer Academic Publishers, 1992.
4. Mohammed Ismail and Terri Fiez, “Analog VLSI Signal and Information Processing “, McGraw Hill, 1994.

S. Y. Kung, H. J. Whilo House, T. Kailath, “VLSI and Modern Signal Processing”, Prentice Hall, 1985.

Program: VLSI Design & Embedded Systems		
Course Title: Standard Cell Design and Layout		Course Code: 17EVEE703
L-T-P: 2-0-1	Credits: 3	Contact Hrs: 4 hrs./week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hrs.: 24	Exam Duration: 03 hrs.	

Chapter No. 1. Introduction to IC Design Flows (08 hrs.)

Use of standard cell elements vs. custom design and Gate array paradigms. Introduction to memory types and construction of memory elements.

Chapter No. 2. Standard cell library composition and usage (08 hrs.)

Types of standard cell elements. Logical and functional elements, primitives and complex macros. Sequential elements and register files. (Flip flop and latch design). Data path elements. Library size vs. usage in standard flows. Drive strength and cell families. Layout of library elements – single height, double height cells. Power Management cells.

Chapter No. 3. Standard cell characterization (08 hrs.)

Usage of standard cells by various tools. Information needed at each stage of design flow. Characterization parameters, setup and runs across PVT corners. Library representation formats. (Gate level simulation, synthesis, timing, layout, timing, LVS, DRC)

References: Standard cell and memory library documentation by Vendors 90nm EDK library

Program: VLSI Design & Embedded Systems		
Course Title: Testing and IC Characterization		**Course Code: 19EVEE704**
L-T-P: 2-0-1	**Credits: 3**	**Contact Hrs.: 4 hrs./week**
ISA Marks: 50	**ESA Marks: 50**	**Total Marks: 100**
Teaching Hrs.: 50	**Exam Duration: 3 hrs.**	

Chapter No. 1. Verification Concepts (10 hrs.)

Concepts of verification, importance of verification, Stimulus vs Verification, functional verification, test bench generation, functional verification approaches, typical verification flow, stimulus generation, direct testing, Coverage: Code and Functional coverage, coverage plan.

Chapter No. 2. System Verilog – Language Constructs (10 hrs.)

System Verilog constructs - Data types: two-state data, strings, arrays: queues, dynamic and associative arrays, Structs, enumerated types. Program blocks, module, interfaces, clocking blocks, modports.

Chapter No. 3. System Verilog – Classes & Randomization (12 hrs.)

SV Classes: Language evolution, Classes and objects, Class Variables and Methods, Class instantiation, Inheritance, and encapsulation, Polymorphism. Randomization: Directed Vs Random Testing. Randomization: Constraint Driven Randomization

Chapter No. 4. System Verilog – Assertions & Coverage (08 hrs.)

Assertions: Introduction to Assertion based verification, Immediate and concurrent assertions. Coverage driven verification : Motivation, Types of coverage, Cover Group, Cover Point, Cross Coverage, Concepts of Binning and event sampling..

Chapter No. 5. Building Testbench (10 hrs.)

Layered testbench architecture. Introduction to Universal Verification Methodology, Overview of UVM Base Classes and simulation phases in UVM and UVM macros. Unified messaging in UVM, UVM environment structure, Connecting DUT- Virtual Interface.

References :

1. System Verilog LRM
2. Chris Spear, Gregory J Tumbush - SystemVerilog for verification - a guide to learning the testbench language features - Springer, 2012
3. Step-by-Step Functional Verification with SystemVerilog and OVM by Sasan Iman SiMantis Inc. Santa Clara, CA Spring 2008 Tools: 1. NC Verilog, NC Sim, VCSMX for System.

Program: VLSI Design & Embedded Systems		
Course Title: Low Power VLSI Circuits		Course Code: 19EVEE705
L-T-P: 2-0-1	Credits: 3	Contact Hours: 4 hrs./week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 40	Examination Duration: 3 hours	

Chapter 1: Introduction to low power VLSI design: (06 hrs.)

Need for Low Power VLSI Chips, sources of power dissipation. Device and Technology impact on Low Power, dynamic power dissipation in CMOS. Power Estimation.

Chapter 2: Power analysis: (05 hrs.)

Simulation Power Analysis, Spice circuits simulator, gate level logic simulator, Probabilistic power analysis

Chapter 3: (05 hrs.)

A new CMOS driver model for transient analysis and power dissipation analysis, low power design of off-chip drivers and transmission lines: a branch and bound approach.

Chapter 4: Different levels of power optimization (07 hrs.)

Low Power Design; circuit Level, logic Level, Low Power Architecture.

Chapter 5: (05 hrs.)

Floor plan design with low power considerations, optimal drivers of high-speed low power ic's, retiming sequential circuits for low power

Chapter 6: Clock Distribution: (04 hrs.)

Low Power Clock distribution, single driver versus distributed buffers. Power management: Power performance management, switching activity reduction, parallel architecture.

Chapter 7: Algorithmic level methodologies for power reduction: (08 hrs.)

Algorithm and architectural level methodologies- algorithmic level analysis & optimization, architecture level estimation and synthesis, Current trends

Text Books

1. Gary K. Yeap, "Practical Low Power Digital VLSI Design", KAP, 2002.
2. Rabaey, Pedram, "Low power design methodologies" Kluwer Academic, 1997.

Reference Books:

1. A. Chandrakasan and R. Brodersen, "Low Power CMOS Design".
2. Sung - Mo Kang & Yosuf Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design", TMH, 2003 (Third Edition).
3. Laung-Terng Wang, Charles E. Stroud, Nur A. Touba, "System-on-chip Test Architectures", 2008.
4. Kaushik Roy, Sharat Prasad, "Low-Power CMOS VLSI Circuit Design" Wiley, 2000.

Program: VLSI Design & Embedded Systems		
Course Title: Internet Of Things		Course Code: 19EVEE706
L-T-P: 2-0-1	Credits: 3	Contact Hours: 4 Hrs./week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hours: 24 Hrs.	Examination Duration: 3 hrs.	

Chapter No. 1: Introduction to IOT (04 hrs.)

Defining IoT, Characteristics of IoT

What is the IoT and why is it important?

Elements of an IoT ecosystem.

Technology and business drivers.

IoT applications, trends and implications.

Physical design of IoT, Logical design of IoT, Functional blocks of IoT, Communication

Chapter No. 2: IoT Architecture: State of the Art (04 hrs.)

History of IoT, M2M – Machine to Machine, Web of Things, IoT protocols

Applications:

Remote Monitoring & Sensing, Remote Controlling, Performance Analysis.

Chapter No. 3: (04 hrs.)

The Layering concepts , IoT Communication Pattern, IoT protocol Architecture, The 6LoWPAN,Security aspects in IoT

Chapter No. 4: IoT Application Development: Application Protocols (06 hrs.)

MQTT, REST/HTTP, CoAP, MySQL

Chapter No. 5: Case Study & Advanced IoT Applications: (06 hrs.)

IoT applications in home, infrastructures, buildings, security, Industries, Home appliances, other IoT electronic equipment's. Use of Big Data and Visualization in IoT, Industry 4.0 concepts.

Hands-on Lab

Arduino, Android and AWS based Experiments

1. AWS Setup and instance creation.
2. Controlling LEDs blinking pattern through UART/WiFi
3. Simple photocell to measure the ambient light level
4. Controlling LEDs blinking pattern through PHP web server.
5. Temperature measurement through ADC and WiFi
6. Controlling and interacting with basic actuators (relay).
7. Android Application development.
8. Controlling of Arduino embedded system using Android App.
9. Motor Speed control using Embedded board and NodeMCU

Lua Programming Based Experiments

1. Introduction to Lua programming
2. Controlling inbuilt LED of ESP8266
3. Controlling Motion Sensor using NodeMCU module.
4. Using ESP8266 as Webserver
    a. Understanding HTML Tags.
    b. Understanding Request.
    c. Reading Parameter Values.
    d. Controlling LED.
5. ThingSpeak Cloud - Data Visualization
    a. Working with Temperature & Humidity Sensor
    b. Working with ThingSpeak Cloud
    c. Posting & Analyzing Sensor Data on ThingSpeak Cloud

Text Books:

1. Arshdeep Bahga, Vijay Madisetti “Internet of Things (A Hands-on-Approach)” Universities Press- 2014.
2. Olivier Hersent, David Boswarthick, Omar Elloumi, “The Internet of Things: Key Applications and Protocols” John Wiley & Sons – 2012.

Reference Books:

Subhas Chandra Mukhopadhyay “Internet of Things Challenges and Opportunities” Springer- 2014.

Program: VLSI Design & Embedded Systems		
Course Code: 20EVEE707	Course Title: AUTOSAR	
L-T-P : 2-0-1	Credits: 3	Contact Hrs.: 4 Hrs./week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
Teaching Hrs.: 40		Exam Duration: 3

Chapter No. 1: AUTOSAR Fundamentals (08 hrs.)

Evolution of AUTOSAR – Motivations and Objectives AUTOSAR consortium – Stake holders – work Packages, AUTOSAR Partnership, Goals of the partnership, Organization of the partnership, AUTOSAR specification, AUTOSAR Current development status, BSW Conformance classes: ICC1, ICC2, ICC3, and Drawbacks of AUTOSAR.

Chapter No. 2: AUTOSAR layered Architecture (07 hrs.)

AUTOSAR Basic software, Details on the various layers , Details on the stacks Virtual Function Bus (VFB) Concept Overview of AUTOSAR Methodology , Tools and Technologies for AUTOSAR AUTOSAR Application Software Component (SW-C) ,Types of SW-components AUTOSAR Run Time Environment (RTE): RTE Generation Process: Contract Phase, Generation Phase, MCAL, IO HW Abstraction Layer, Partial Networking, Multicore, J1939 Overview, AUTOSAR Ethernet, AUTOSAR E2E Overview , AUTOSAR XCP, Metamodel , From the model to the process , Software development process.

Chapter No. 3: Methodology of AUTOSAR and Communication in AUTOSAR (10 hrs.)

CAN Communication, CAN FD, CANape, Application Layer and RTE, intra and inter ECU communication, Client-Server Communication, Sender-Receiver, Communication, CAN Driver, Communication Manager (ComM), Overview of Diagnostics Event and Communication Manager

Chapter No. 4: Overview about BSW constituents (05 hrs.)

BSW Constituents: Memory layer, COM and Services layer, ECU abstraction, AUTOSAR, Operating system, Interfaces: Standard interface, AUTOSAR standardized interface, BSW-RTE interface,(AUTOSAR interface), BSW-ECU hardware interface, Complex device drivers and BSW module configuration, AUTOSAR Integration.

Chapter 5: MCAL and ECU abstraction Layer (05 hrs.)

Microcontroller Drivers, Memory drivers: on-chip and off chip drivers, IO drivers(ADC, PWM, DIO), Communication drivers: CAN driver, LIN drivers, Flexrfay

Chapter 6: Service Layer (05 hrs.)

Diagnostic Event Manager, Function inhibits Manager, Diagnostic communication manager, Network management, Protocol data unit router, Diagnostic log and trace unit, COMM manager.

Text Book (List of books as mentioned in the approved syllabus)

1. Ronald K. Jurgen, Infotainment systems, 2007, SAE International, 2007

Program: VLSI Design & Embedded Systems		
Course Title: Mini Project		**Course Code: 19EVEW701**
L-T-P-SS: 0-0-3	**Credits: 3**	**Contact Hours: 6**
CIE Marks: 50	**SEE Marks: 50**	**Total Marks: 100**
	Examination Duration: 3 hours	

1. The project needs to encompass the concepts leant in a courses in the previous semesters, so that the student will learn to integrate, the knowledge acquired to provide a solution to the defined problem statement of the mini-projects.
2. Student can select a project which leads to a product or model or prototype related to following areas (not limited to these areas).
    1. Embedded systems
    2. MEMS
    3. VLSI design
    4. Image processing
    5. Micro controllers
    6. Communications
3. Time plan: Effort to do the project should be between 50 hours,

Semester End Evaluation (SEE)

Semester end examination (SEE) includes submission of the project report, demonstration of the mini-projects and viva-voce conducted by the external and internal examiner. SEE carries 50% weightage of total marks of mini-projects.

Semester: III Semester M.Tech.

Program: VLSI Design & Embedded Systems		
Course Title: Internship / Mini Project		**Course Code: 17EVEI801**
L-T-P: 0-0-8	**Credits: 8**	**Contact Hours: 16/week**
ISA Marks: 50	**ESA Marks: 50**	**Total Marks: 100**
	Examination Duration: 3 hours	

Internship: 6 weeks of training in any reputed industry. A report has to be made and should be submitted at the end of the training.

OR

Mini-Project 3:

1. The project needs to encompass the concepts leant in a courses in the previous semesters, so that the student will learn to integrate, the knowledge acquired to provide a solution to the defined problem statement of the mini-projects.
2. Student can select a project which leads to a product or model or prototype related to following areas (not limited to these areas).
    1. Embedded systems
    2. MEMS
    3. VLSI design
    4. Image processing
    5. Micro controllers
    6. Communications

Semester End Evaluation (ESA)

Semester end examination (ESA) includes submission of the project report, demonstration of the mini-projects and viva-voce conducted by the external and internal examiner. ESA carries 50% weightage of total marks of mini-projects.

Program: VLSI Design & Embedded Systems		
Course Title: Project Phase I / Minor Project		Course Code: 17EVEW801
L-T-P: 0-0-10	Credits: 10	Contact Hours: 20/week
ISA Marks: 50	ESA Marks: 50	Total Marks: 100
	Examination Duration: 3 hours	
12 weeks duration shall be carried out. Candidates in consultation with the guides shall carryout literature survey / visit to Industries to finalize the topic of dissertation. Evaluation of the same shall be taken up during end of III Semester.		

Semester: IV Semester M.Tech

Program: VLSI Design & Embedded Systems		
Course Title: Project Phase II / Major project		**Course Code: 17EVEW802**
L-T-P: 0-0-20	**Credits: 20**	**Contact Hours: 40 /week**
ISA Marks: 50	**ESA Marks: 100**	**Total Marks: 150**
	Examination Duration: 3 hours	
24 weeks duration. Evaluation shall be taken during the end of the IV Semester. Need to present three reviews during the project work. Evaluation shall be taken up during the end of IV Semester. At the end of the Semester Project Work Evaluation and Viva-Voce Examinations will be conducted.		